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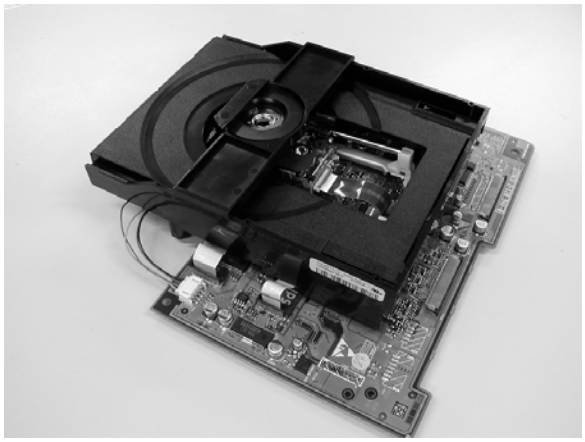

Service Manual

CLASS 1
LASER PRODUCT

DVD VIDEO

COMPACT disc DIGITAL VIDEO

COMPACT disc DIGITAL AUDIO

Contents **Page**

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PHILIPS

1. Technical Specifications

1.1 Interfaces and Pin Assignments

SD4 00_SA CH supports both configurations of single-disc and 5-disc changer SACD player.
In table 1-1, interfaces or connectors stuffing options are given for applications of single-disc and 5-disc changer.

Table 1-1 Interfaces or connectors stuffing options

Disc Type	1100	1300	1301	1302	1500	1701	1702	1703	1704	1900	1012	1013
Single-disc	√	√	√	√	√		√	√	√			√
5-disc	√	√	√		√	√	√	√	√	√		√

The interfaces or connectors are placed on both PCB layers of top and bottom as shown in figure 1-1 and figure 1-2 respectively.

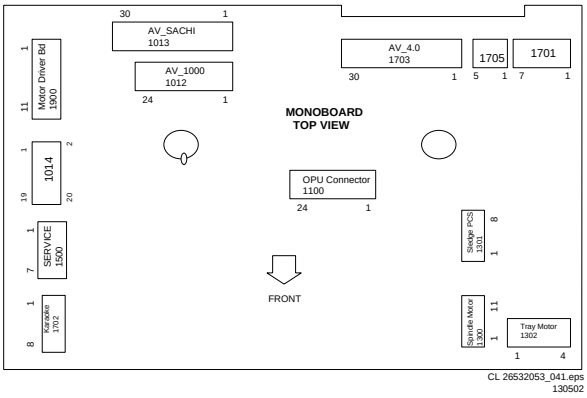


Figure 1-1 Interfaces placement on PCB top layer

Connector 1705 is an option for the usage of SACD1000 set only for connecting monoboard to front panel board. Connector 1701 is also an option for the monoboard power supply 12V/ 5V/3V3 in case of the requirements needed for further improvement on audio performance of SACD.
Connector 1014 is for either DCU (Diagnostic Controller Unit) or BST (Boundary Scan Test) used by industrial only.

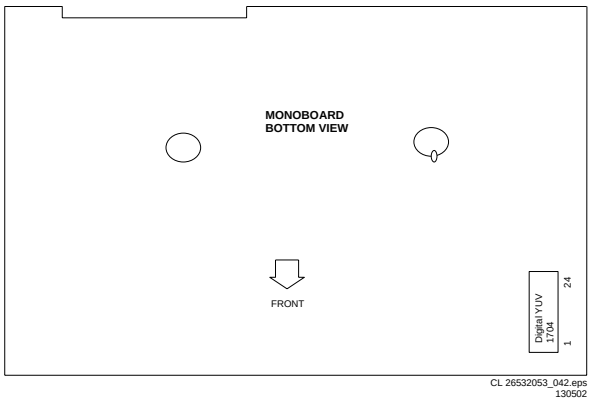


Figure 1-2 Interfaces placement on PCB bottom layer

1.2 Connections

1.2.1 Interface AV_4.0 at Location 1703:

1.	I^2C_SCL/SIODATA	I^2C SCL
2.	I^2C_SDA/SIOCLK	I^2C SDA
3.	SCART1	low blanking 1 (0/6/12V)
4.	SCART0	low blanking 0 (0/6/12V)
5.	B_REF	GND
6.	B_U	B_output
7.	G_REF	GND
8.	G_Y	G_output
9.	R_REF	GND
10.	R_V	R_output
11.	Y_REF	GND
12.	Y	Y_output
13.	C_REF	GND
14.	C	C_output
15.	CVBS-REF	GND
16.	CVBS	CVBS output
17.	+3V3	Power supply +3V3
18.	+3V3	Power supply +3V3
19.	+5V	Power supply +5V
20.	+12V	Power supply +12V
21.	+12V	Power supply +12V
22.	MUTE	Analogue output Mute
23.	GND	GND
24.	PCMSCLK	PCM Bit clock
25.	PCMDATA0	PCM data 0
26.	GND	GND
27.	PCMCLK	PCM Clock
28.	PCMLRCLK	PCM Word clock
29.	GND	GND
30.	SPDIF	SPDIF outpu

1.2.2 Optional Interface AV_1000 at Location 1012:

1.	GND	GND
2.	384FS 16.9344MHz	DAC mastering clock
3.	GND	GND
4.	SEL_PCM/ DSD_LFE	LFE channel (Ch-3)
5.	GND	GND
6.	DATA_CeLf/ DSD_CENTRE	Front Centre channel (Ch-2)
7.	GND	GND
8.	SEL_PCM/DSD_Rs	Right surround (Ch-5)
9.	GND	GND
10.	DATA_LsRs/DSD_Ls	Left surround (Ch-4)
11.	GND	GND
12.	SEL_PCM/DSD_RIGHT	Front Right Channel (Ch-1)
13.	GND	GND
14.	DATA_LeRi/DSD_LEFT	Front Left Channel (Ch-0)
15.	GND	GND
16.	WORK_CLK/SEL_DSD	DSD stereo
17.	GND	GND
18.	BIT_CLK/DSD_CLK	DSD clock
19.	GND	GND
20.	256FS	Audio Clock FS=32KHz, 44.1KHz, 48KHz and 96KHz
21.	GND	GND
22.	SCL-DAC	I^2C SCL for DAC
23.	SDA-DAC	I^2C SDA for DAC

24.	GND	GND

1.2.3 Optional Power Supply Connector at Location 1701:

1.	+3V3	Power supply +3V3
2.	+3V3	Power supply +3V3
3.	+5V	Power supply +5V
4.	GND	Ground
5.	GND	Ground
6.	MGND	Power ground
7.	+12V	Power supply +12

1.2.4 Optional Connector of Sacd1000 Set (From Monoboard to Front Panel) at Location 1705:

1.	SCL	I^2C SCL
2.	GND	Ground
3.	SDA	I^2C SDA
4.	STB_CONT	Standby Control
5.	P50	Project P5

1.2.5 Interface AV_SACHI at Location 1013:

1.	GND	GND
2.	384FS	DAC mastering clock 16.9344MHz
3.	GND	GND
4.	SEL_PCM/DSD_LFE	LFE channel (Ch-3)
5.	GND	GND
6.	DATA_CeLf/DSD_CENTRE	Front Centre channel (Ch-2)
7.	GND	GND
8.	SEL_PCM/DSD_Rs	Right surround (Ch-5)
9.	GND	GND
10.	DATA_LsRs/DSD_Ls	Left surround (Ch-4)
11.	GND	GND
12.	SEL_PCM/DSD_RIGHT	Front Right Channel (Ch-1)
13.	GND	GND
14.	DATA_LeRi/DSD_LEFT	Front Left Channel (Ch-0)
15.	GND	GND
16.	WORK_CLK/SEL_DSD	DSD stereo
17.	GND	GND
18.	BIT_CLK/DSD_CLK	DSD clock
19.	GND	GND
20.	256FS	Audio Clock FS=32KHz, 44.1KHz, 48KHz and 96KHz
21.	GND	GND
22.	SCL-DAC I2C	SCL for DAC
23.	SDA-DAC I2C	SDA for DAC
24.	GND	GND
25.	PCMDATA3/DSD_PCM8	Option 1:PCMDATA3 Option 2: DSD_Ch7
26.	GND	GND
27.	P50	P50 (I2C Slave Data Available Interrupt)
28.	GPIO2	General I/O port 2 Option 1 : Supporting 3 control line type DAC, DAC_CLK
29.	GPIO3	General I/O port 3 Option 1: Supporting 3 control line type DAC, DAC_DATA
30.	GPIO1	General I/O port Option 1: Supporting 3 control line type DAC, DAC_C

1.2.6 Karaoke Interface at Location 1702:

1.	KOKSCLK	Karaoke PCM bit clock (I2S format)
2.	+12V	Power Supply +12V
3.	KOKLRCLK	Karaoke PCM left-right / word clock (I2S format)
4.	GND	Ground
5.	KOKDATA	Karaoke PCM data (I2S format)
6.	GND	Ground
7.	KOKPCMCLK	Karaoke PCM system clock (I2S format)
8.	KOKVOCDET	Karaoke vocal detect signal

1.2.7 Digital YUV Interface at Location 1704:

1.	GND	Ground
2.	SDA	I2C SDA
3.	SCL	I2C SCL
4.	Odd/Even	
5.	HSYNC	Horizontal Sync
6.	GND	Ground
7.	27MHz Clock	27MHz Clock
8.	GND	Ground
9.	YC0	Digital video bit 0
10.	GND	Ground
11.	YC1	Digital video bit 1
12.	GND	Ground
13.	YC2	Digital video bit 2
14.	GND	Ground
15.	YC3	Digital video bit 3
16.	+5V	Power Supply +5V
17.	YC4	Digital video bit 4
18.	+3V3	Power Supply +3V3
19.	YC5	Digital video bit 5
20.	+3V3	Power Supply +3V3
21.	YC6	Digital video bit 6
22.	GND	Ground
23.	YC7	Digital video bit 7
24.	GND	Ground

1.2.8 Service connector at Location 1500:

1.	TXD_SER	TXD service UART
2.	SERVICE	Service or normal mode select
3.	RXD_SER	RXD service UART
4.	RTS_SER	Not used (RTS service UART)
5.	GND	Ground
6.	CTS_SER	Not used (CTS service UART)
7.	+5V_SER	Positive 5V (isolated from internal +5V by ferrite bead

1.2.9 To Motor Driver Board Interface at Location 1900:

1.	TBL-POS	Carousel Rotation Position Detection
2.	I2CSCL	I2C Clock
3.	I2CSDA	I2C Data
4.	GND	Ground
5.	Clockwise_CM	Carousel Clockwise Rotation Control
6.	Counterclockwise_CM	Carousel Counterclockwise Rotation Control
7.	+5V	+5V Power Supply
8.	GND	Ground
9.	+12V	+12V Power Supply
10.	+12V	+12V Power Supply
11.	GND	Ground

1.3 Signal Specifications

This the specification of all signals as described under "Connections"
H = +5V ±0.5V
h = 3V3 ±0.3V
L = 0V ±0.5V
l = 0V ±0.3V

Stby	:	There is no standby mode at module level. The module operate in power-off and power-on only.
Standby control line	:	Not available on module level.
P50	:	Connection between front and A/V board, and can be used as P50 signal line.
	:	The signal is not connected to the module electronics.
Slow blanking scart	:	This signal has three levels which depend on the level of the output ports SCART0 and SCART1. It will be converted by the external board to 0/6/ 12 voltage level use for scart function switching.
Audio mute	:	Can be used for audio mute transistors during stop or power On/Off.
	:	Mute on : 3V3 ±0V3
	:	Mute off: 0V ±0V3
I2S data0 out	:	I2S front data output.
	:	Level - h / l
I2S wordselect / I2S bitclock	:	I2S timing signals
	:	Level - h / l
I2S systemclock	:	256xFS audio systemclock.
	:	Level - h / l
Clockwise/Counterclockwise_CM	:	Carousel output for 5-Disc changer
	:	Level - h / l
TBL_POS	:	Position sensor for carousel rotation of 5-disc changer
	:	Level - h / l
LFE_SEL	:	Low frequency effect selection for the A/V board.
	:	LFE_SEL_low - l
	:	LFE_SEL_high - h
Center_on	:	Switches the center audio to the scart output.
	:	Center to scart - h
	:	L/R to scart - l
Karaoke	:	I2S input - h / l
	:	PCMCLK output - h / l
SPDIF out	:	Digital audio output level - H / L
Hor. Sync	:	Video Horizontal synchronisation
	:	Level - h / l
DSD/PCM output	:	Digital output for High End DAC
	:	Level - h / l
I^2C clock / I^2C data	:	I^2C databus
	:	Level - H / L at modules connectors
TXD / RXD / RTS / CTS	:	Service UART to be connected direct to PC serial input.
	:	Output levels - H / L
	:	Input levels RS232 compliant
Service activation	:	To activate service mode, this line is tied to GND

1.4 Performance:

1.4.1 Digital Output

CDDA/LPCM	:	according IEC60958
MPEG1 is converted to LPCM	:	
MPEG2, AC3 audio.MP3	:	according IEC1937
DTS.	:	according IEC61937 amendment 1.
	:	Digital output level is 0V / 5V with GND as reference. To meet the standards a decouple circuit is necessary.

1.4.2 I2S Output

Resolution	:	Up to 24bit.
Sample rate	:	32kHz / 44.1kHz / 48kHz / 64kHz / 88.2kHz / 96kHz / 128kHz / 176.4kHz / 192kHz.
Standard	:	Philips I2S output
Number of I2S outputs	:	Basic 6 channels: Front / Surround / Center-LFE.
	:	Additional 2 channels: downmix stereo
Deemphasis	:	Internally processed by the module.
Audio source streams	:	PCM / LPCM /MPEG1 / MPEG2 / AC3 / MP3 / DTS / MLP.
Audio processing	:	Dolby ProLogic decoder / Dolby surround downmix / SRS TruSurround / Circle Surround / TruBass.

1.4.3 Analog Audio

The module has no analog audio ouput.	:	The analog audio specification will be determined by the external DAC circuit.

1.4.4 Video.

Standards	:	The video output standard will follow the source material.
	:	The OSD standard is switchable between PAL or NTSC.
Outputs	:	The module has 6 analog outputs in 4 formats: Y/C; CVBS; RGB / YUV. RGB / YUV component video signals share the same lines. Therefore, the module

is unable to output both RGB and YUV simultanious.

Specification. : The output comply fully with [PQR-IMS] Class III.

: DC level - sync bottom at 0.43V ±10% (100% white) and 0.9V ±10% (black).

: Output impedance - 75Ohm.

: The following specification points are significantly better then [PQR_IMS]

: SNR on all video outputs is better then 65dB.

: Video bandwidth - 8MHz (±3dB) / 16MHz (±3dB) for STi5588 progressive scan.

2. Safety Instructions, Warnings, and Notes

2.1 Safety Instructions

2.1.1 General Safety

Safety regulations require that during a repair:
- Connect the unit to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol ▲, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.

Safety regulations require that after a repair, you must return the unit in its original condition. Pay, in particular, attention to the following points:
- Route the wires/cables correctly, and fix them with the mounted cable clamps.
- Check the insulation of the mains lead for external damage.
- Check the electrical DC resistance between the mains plug and the secondary side:
  1. Unplug the mains cord, and connect a wire between the two pins of the mains plug.
  2. Set the mains switch to the 'on' position (keep the mains cord unplugged!).
  3. Measure the resistance value between the mains plug and the front panel, controls, and chassis bottom.
  4. Repair or correct unit when the resistance measurement is less than 1 MΩ.
  5. Verify this, before you return the unit to the customer/ user (ref. UL-standard no. 1492).
  6. Switch the unit 'off', and remove the wire between the two pins of the mains plug.

2.1.2 Laser Safety

This unit employs a laser. Only qualified service personnel may remove the cover, or attempt to service this device (due to possible eye injury).

Laser Device Unit

Type	:	Semiconductor laser GaAlAs
Wavelength	:	650 nm (DVD)
	:	780 nm (VCD/CD)
Output Power	:	20 mW (DVD+RW writing)
	:	0.8 mW (DVD reading)
	:	0.3 mW (VCD/CD reading)
Beam divergence	:	60 degree

Figure 2-1

Note: Use of controls or adjustments or performance of procedure other than those specified herein, may result in hazardous radiation exposure. Avoid direct exposure to beam.

2.2 Warnings

2.2.1 General

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ⚠). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are at the same potential as the mass of the set by a wristband with resistance. Keep components and tools at this same potential. Available ESD protection equipment:
  – Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and earth cable) 4822 310 10671.
  – Wristband tester 4822 344 13999.
- Be careful during measurements in the live voltage section. The primary side of the power supply (pos. 1005), including the heatsink, carries live mains voltage when you connect the player to the mains (even when the player is 'off'!). It is possible to touch copper tracks and/or components in this unshielded primary area, when you service the player. Service personnel must take precautions to prevent touching this area or components in this area. A 'lightning stroke' and a stripe-marked printing on the printed wiring board, indicate the primary side of the power supply.
- Never replace modules, or components, while the unit is 'on'.

2.2.2 Laser

- The use of optical instruments with this product, will increase eye hazard.
- Only qualified service personnel may remove the cover or attempt to service this device, due to possible eye injury.
- Repair handling should take place as much as possible with a disc loaded inside the player.
- Text below is placed inside the unit, on the laser cover shield:

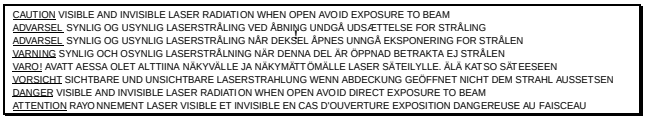


Figure 2-2

2.2.3 Notes

Dolby

Manufactered under licence from Dolby Laboratories. "Dolby", "Pro Logic" and the double-D symbol are trademarks of Dolby Laboratories. Confidential Unpublished Works. ©1992-1997 Dolby Laboratories, Inc. All rights reserved.

Figure 2-3

Trusurround

TRUSURROUND, **SRS** and symbol (fig 2-4) are trademarks of SRS Labs, Inc. TRUSURROUND technology is manufactured under licence frm SRS labs, Inc.

Figure 2-4

3. Directions for Use

There is no DFU available

4. Mechanical Instructions

4.1 Dismantling Instruction

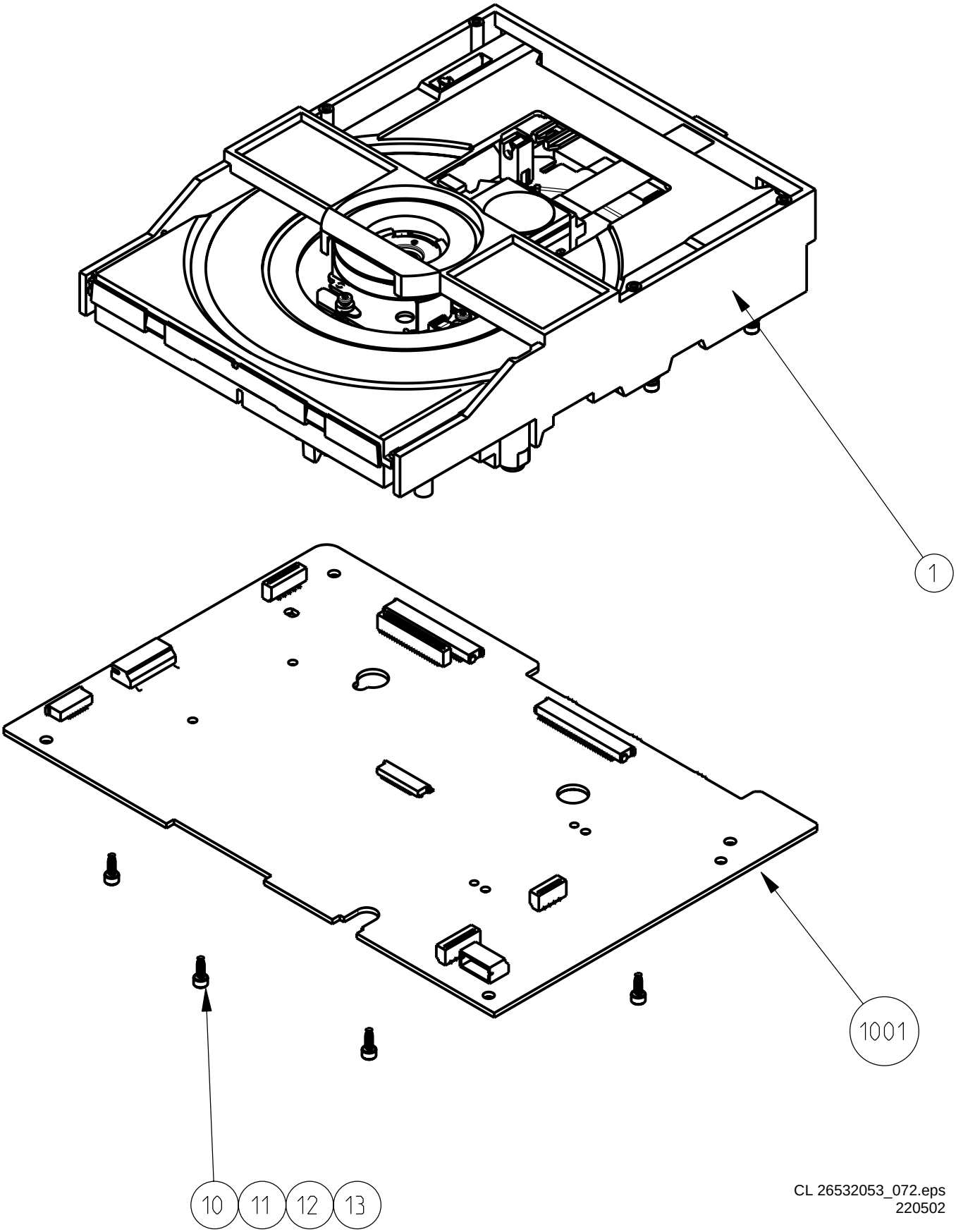


Figure 4-1

4.1.1 Dismantling of DVD Mono Board

1. See Figure 4-1 for dismantling of DVD module.

2. Unlock the OPU conn 1100, Sledge motor conn 1301 and disc motor conn 1300 and remove the Flex connections.

3. Remove the wire connection to Tray motor conn 1302.

4. Remove 4 screws 10 to 13.

5. Remove the Mono Board

Note: Flex cables are very fragile,care should be taken during dismounting and when mounting,ensure that Flex cables are inserted properly into the Flex socket and locked.

4.1.2 Opening of Tray Manually

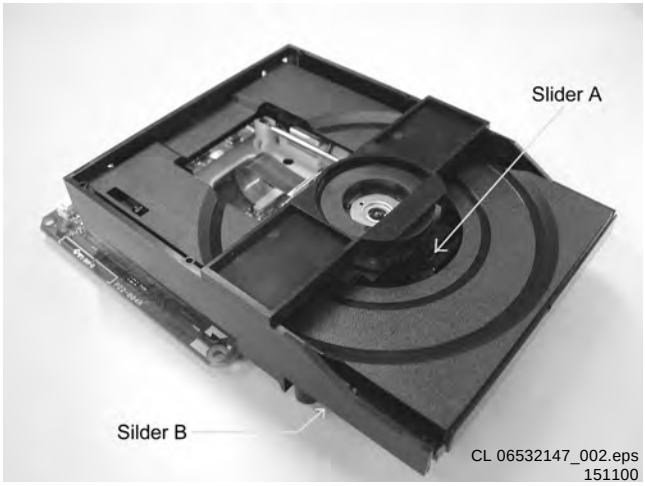


Figure 4-2

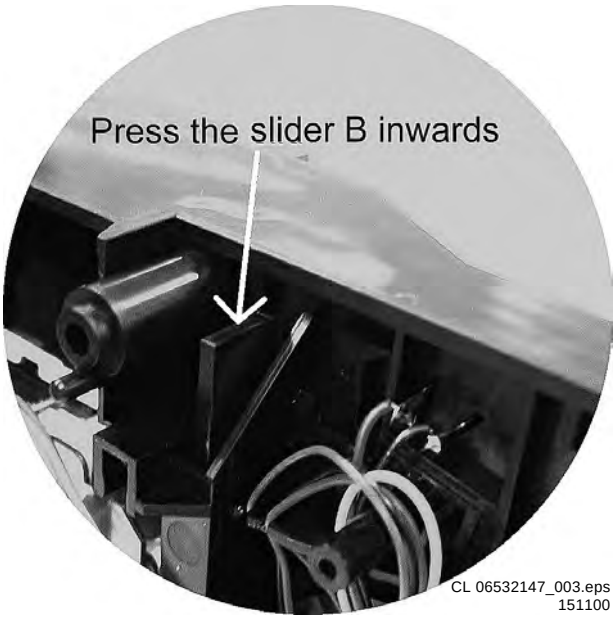


Figure 4-3

It is possible to open the tray manually by moving the Slider in the position as shown in Figure 4-2 and Figure 4-3
When the slider A is not accessible when a disc is loaded, unlock the tray by pressing the slider B inward as shown in Figure 4-3.The Tray is now disengaged and can be pulled outwards.

When no disc is loaded, unlocking the Tray can also be done by moving the Slider A in the direction as shown in Figure 4-4 and pull the Tray outwards.

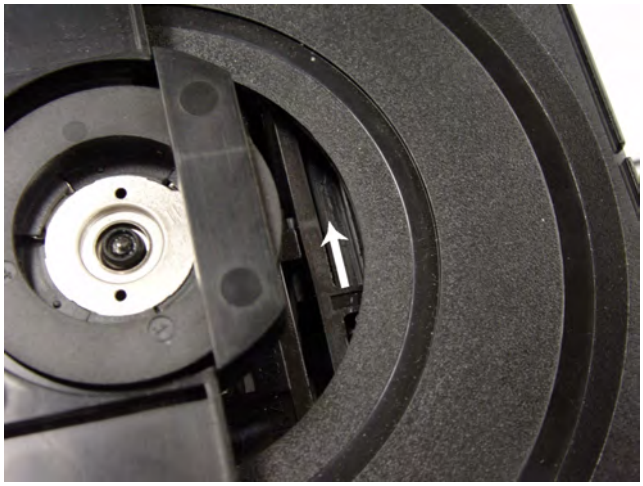


Figure 4-4

4.2 Service Hints

4.2.1 DVD Module

This module can be repaired as follows:

1. The VAL6011/14 is a combination of loading mechanism and DVD-mechanism. Both the mechanism is not a repairable unit and in case of failure it has to be replaced with a new loader VAL6011/14.

   Note: When replacing with a new VAL6011/14 two solder joints have to be removed after connecting the OPU flex foil to the board.
   The solder joints which shortcircuits the laser diodes to ground are for protection against ESD. Refer to Figure 4-5 and Figure 4-6 for location of solder points.

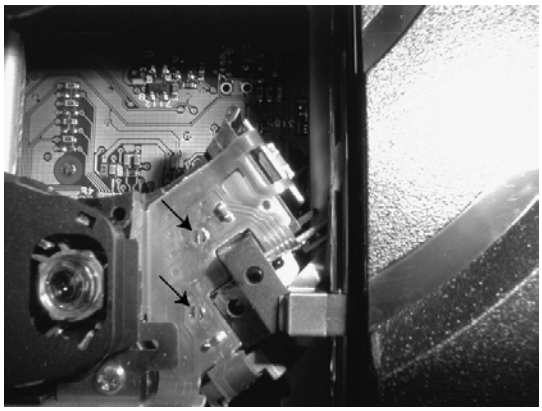


Figure 4-5

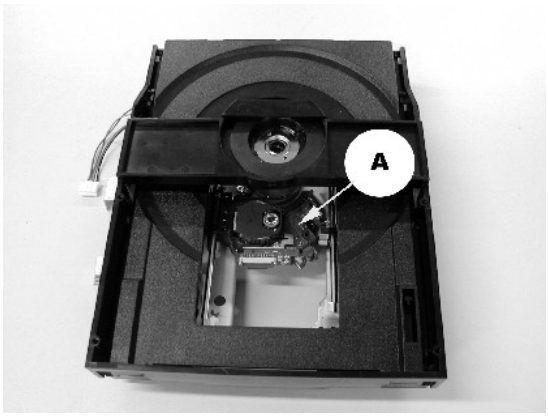


Figure 4-6

2. The mono board has to be repaired down to component level. Repair handling of the monoboard requires a workshop with sophisticated desoldering tools.

5. Test Instructions Mono Board DVD-SD4.00SA_CH

5.1 General

- Impedance of measuring-equipment should be > 1MΩ.
- Most tests have to be done by software commands. Together with the software command you will find a Ref.# nbr. This is the number of the diagnostic nulceus used for this test. More detailed information can be find in the chapter “Diagnostic Nuclei”.
- Levels: Most measurements are digital measurements. The signal levels specification in this document are defined as follows:
  low:< 0.3V
  high:> 3.0V
  LOW:< 0.4V
  HIGH:> 4.5V
- All the waveforms measurement carried out in these test instruction will be base on the testpoint indicated in the Monoboard schematic diagram in the service manual.

5.2 General Start-up Measurements

5.2.1 Supply Check:

Table 5-1 Supply check

Testpoint	Supply	Used by
F781	+3V3	Main supply voltage
F782	+5V	Main supply voltage
F783	+12V	Main supply voltage
F710	+3V3SA	Analog 3V3 front-end circuitry
F711	+3V3SD	Digital 3V3 front-end circuitry
F785	FUR-3V3	Digital 3V3 Furore2 interface circuitry
F784	+3V3ST	Digital 3V3 back-end circuitry
F724	3V3D	Digital 3V3 cicuitry
F787	FUR-1V8	Digital 1V8 Furore2 core circuitry
F786	VDDA-FUR	Analog 1V8 Furore2 circuitry
F717	+5VSA	Analog 5V front-end circuitry
F715	+5VSD	Digital 5V front-end circuitry
F721	+5VAV	Analog 5V back-end circuitry
F718	+5VD	Digital 5V back-end circuitry
F727	VDDSTA	Analog STi 55xx circuitry
F729	VDDSTC	Core STi 55xx circuitry
F725	VDDSTD	Digital STi 55xx circuitry

STi 55xx uses various power supply voltages that depend on which processor is being used

Table 5-2 Back-end processor

Back-end Processor	VDDSTA (Analog)	VDDSTC (Core)	VDDSTD (Digital)
STi 5580	+2V5	+2V5	+2V5
STi 5588	+1V8	+1V8	+3V3
STi 5519	+2V5	+2V5	+2V5

The module operates in power-off and power-on only. There is no standby mode at module level. In power-off, the module does not response to any communication or signals.
Before starting the measurement, ensure that all power supply are connected to the monoboard via connector 1703 or 1701 and that the PC interface cable is connected to the Service interface connector 1500 of the monoboard.

5.2.2 Reset Check:

To ensure a proper start-up of the monoboard, the back-end reset signal RESETn is required at the STi55xx input (testpoint F906) after power-on.
To check the reset timing, measure the RESETn (testpoint F906) and the +3V3ST supply (testpoint F784), reset circuit trigger signal.

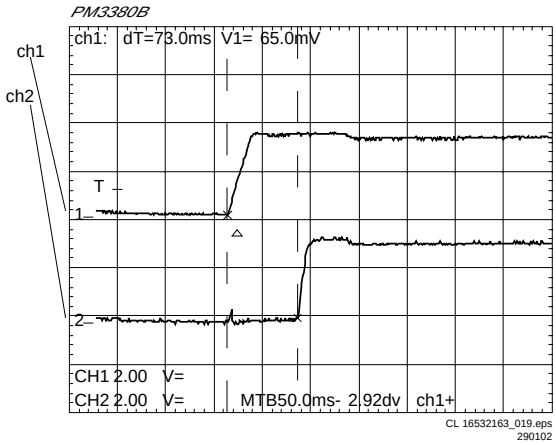


Figure 5-1 Reset

Nb: The RESETn rising edge should be at least 100msec after the +3V3ST (refer to Figure 5-1).
If the reset input does not go high then check the reset circuit around transistor 7409.

5.2.3 Clock Check

To check the correct functioning of the STI55xx, we first have to check the presence of all clocks.
All clocks to be measured with 0.02% tolerance.

Table 5-3 Clock check

Name	Testpoint	Frequency	Waveform
384FS	F042	16.9344MHz	Refer to Fig 5-3
27M_CLK_ST	F932	27MHz	Refer to Fig 5-2
PCM_CLK_ST	F885	11.2896MHz	Refer to Fig 5-5
Audio_CLK	F935	11.2896MHz	Refer to Fig 5-5
Iguana_CLK	F207	8.4672MHz	Refer to Fig 5-4

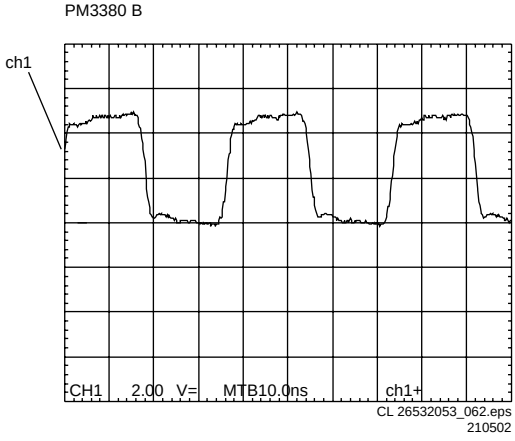


Figure 5-2 27M_CLK

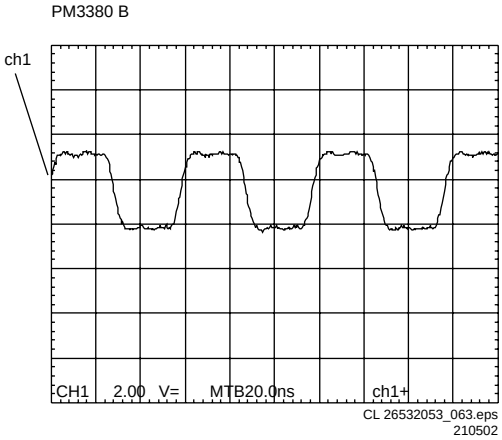


Figure 5-3 384FS

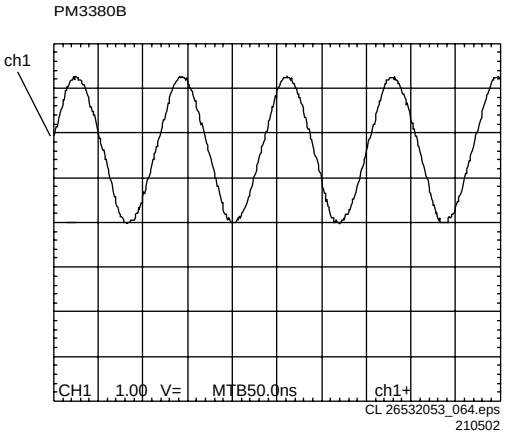


Figure 5-4 Iguana_CLK

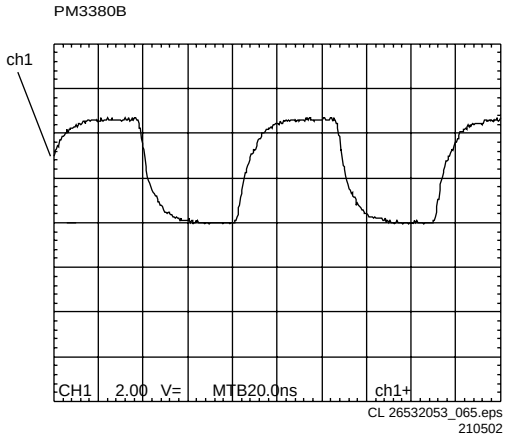


Figure 5-5 PCM_ST_CLK / Audio_CLK

5.3 µP Environment:

5.3.1 General:

All the tests are carried out by software tests. To start the software tests, connect a PC to the serial bus of the STI55xx. Use connector 1500 for this connection:

Table 5-4 PC connection

Connector pin	Signal
1500-1	TXT_SER (STi55xx out)
1500-2	SERVICE-mode select
1500-3	RXD_SER (STi55xx in)
1500-4	RTS_SER (Not in use)
1500-5	GND
1500-6	CTS_SER (Not in use)
1500-7	+5V_SER

Now start the terminal program. Make sure that the service-pin (pin 1500-2) of the µP is pulled low.
The terminal program of your PC should now display: “DVDv4 Diagnostic software version ...”. This message already means that the µP is running. The first 5 commands from the diagnostic software will be carried out automatically during diagnostic start-up. The other commands can be carried out by selecting the “command input” and simply type the reference nbr. to do the test or select the “Menu - driven” test.
To be sure that the µP is able to run the diagnostic software, serial port will be checked during start-up.

Table 5-5 Serial port check

Ref. #	Reference Name	Remark
(1)	BasicSpAcc	Serial port Access test/ initialisation
(2b)	BasicInterconSdram	Check SDRAM interconnection with CPU
(4)	BasicSdramWrR	Check Basic SDRAM memory

With this test, the serial communication is checked in both directions.

5.3.2 Memory Check:

The μP has a data bus that is connected to a Flash and also internal link to the MPEG SDRAM inteface.
At start-up,the SDRAM bus is checked

Table 5-6 Memory check

Ref. #	Command Name	Remark
(2b)	BasicInterconSDRAM	Data and address bus Interconnection
6	PapChksFl	Checksum FLASH
16	CompSdramWrR	SDRAM Write Read

CompSdramWrR checks the complete SDRAM for failures inside the IC.The BasicInterconSDRAM check is done by writing & reading some well chosen patterns to all address and data interconnections of the SDRAM.
The PapChksFl calculate and verify checksum of the FLASH. This includes the binary file checksum and the four modules.

5.4 General I/O Port & Peripherals Check

5.4.1 I^2C Bus / EEprom Check

To access the EEprom, the I2C bus is used. So by writing and reading to the EEprom the chip and the bus is checked. With next commands a certain byte is written to the EEprom. The original information will always be written back into the EEprom.

Table 5-7 EEprom check

Ref. #	Command Name	Remark
11	PapI2cNvram	I2C NVRAM access

The complete Eeprom can also be checked on failures by writing to all addresses and reading back. This test takes a long time (110 sec).

Table 5-8

Ref. #	Command Name	Remark
15	PapNvramWrR	NVRAM Write Read

5.4.2 Audio Clock Switch Check

The internally generated Audio clock can be set to either 44.1 kHz (CD_DA), 48 kHz (DVD) or 96 kHZ (DVD). To check the different mode, use the following commands and measure the waveform as correct operation cannot be detected by the Diagnostic Software.

Table 5-9 Audio clock switch check

Ref #	Command Name	Remark	Test point	Frequency
7a	PapUclkAclkCdda	μClock A_CLK in 44.1kHz mode(Fig 5-4)	T885	11.2896MHz 0.02%
7b	PapUclkAclkDvd	μClockA_CLK in 48kHz mode (Fig 5-5)	T885	12.288MHz 0.02%
7c	PapUclkAclkDvd96	μClock A_CLK in 96kHz mode (Fig 5-6)	T885	24.576MHz 0.02%

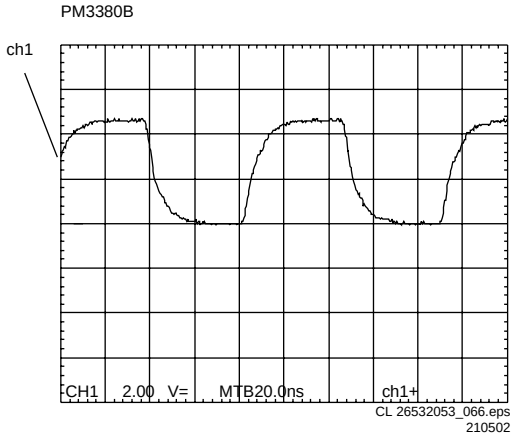


Figure 5-6 μClock A_CLK in 44.1kHz mode

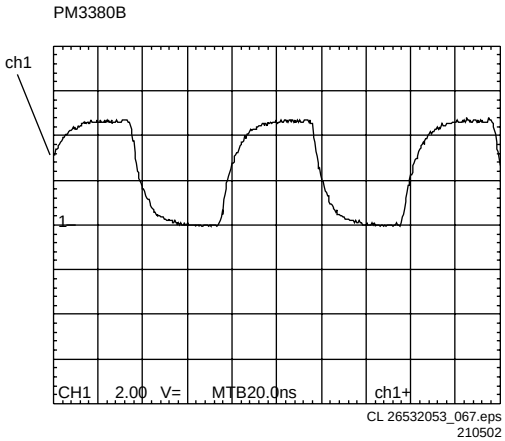


Figure 5-7 μClockA_CLK in 48kHz mode

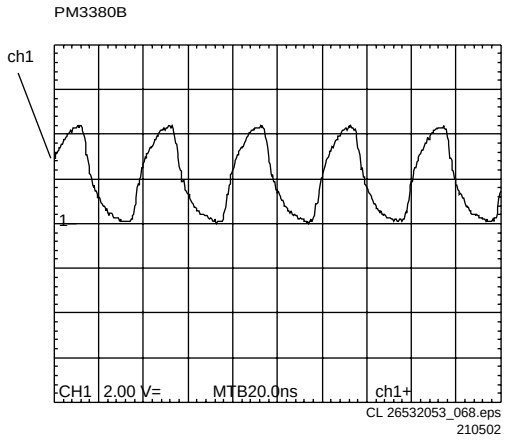


Figure 5-8 μClock A_CLK in 96kHz mode

5.4.3 Audio Mute Check

Switch on the Mute circuit by sending next command:

Table 5-10 Audio mute check

Ref. #	Command Name	Remark
19a	AudioMuteOn	AudioMuteOn

Check the Mute output again at testpoint T798: 3V3 ±10%
Switch off the Mute circuit by sending next command

Table 5-11 Audio mute check

Ref. #	Command Name	Remark
19a	AudioMuteOff	AudioMuteOff

Check the Mute output at testpoint T798: 0V ±0.3V

5.4.4 Audio I2S Check

To check the audio output, connect a audio DAC (on the A/V board) to the I2S output and start-up the audio test. Look at the audio outputs from the A/V board for both sine and pink noise.

Table 5-12 Audio I2S check

Ref. #	Command Name	Remark	Audio outputs
21a	AudioSineOn	Audio Sine signal Off	Audio Sine signal On Sine, 1kHz on stereo Press stop button
20a	AudioPinkNoiseOn	Audio Pinknoise On	Pink Noise on 6 channels
20b	AudioPinkNoiseOff	Audio Pinknoise Off	

The audio signal (sine or pink noise) will also be present on the digital ouput (SPDif). This can be checked by connecting an amplifier with digital input.
Check the I2S output.

Table 5-13 NameTestpointWaveform

Name	Testpoint	Waveform
PCMLRCLK	F886 / F021	Refer to Figure 5-9
PCMSCLK	F883 / F019	Refer to Figure 5-10
PCMDATA0	F884	Refer to Figure 5-11
DATA_LR/DSD_LEFT	F025	Refer to Figure 5-11
DATA_LsRs/DSD_Ls	F029	Refer to Figure 5-11
DATA_CL/DSD_CENTRE	F034	Refer to Figure 5-11
PCMCLK	F885 / F016	Refer to Figure 5-12
SPDIF	F719	Refer to Figure 5-13

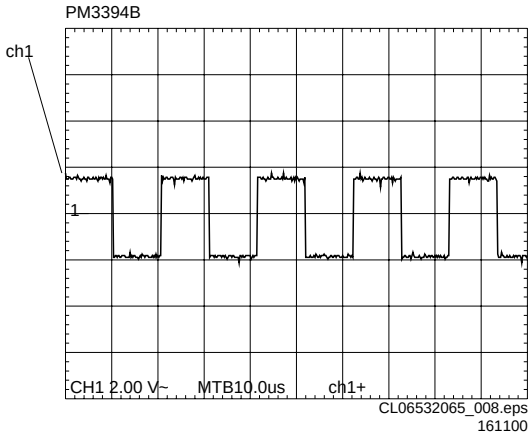


Figure 5-9 PCMLRCLK

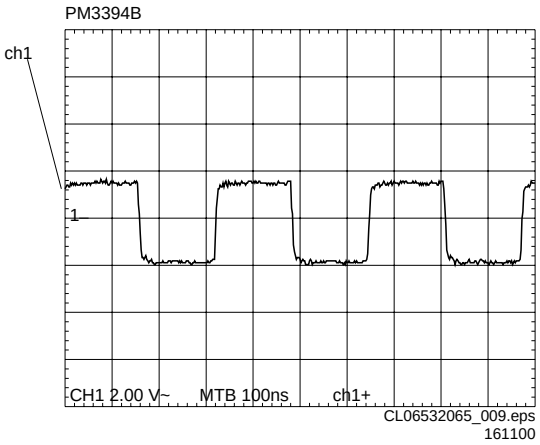


Figure 5-10 PCMSCLK

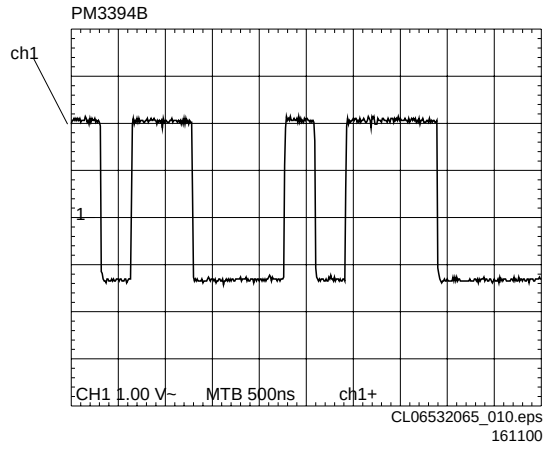


Figure 5-11 PCMDATA

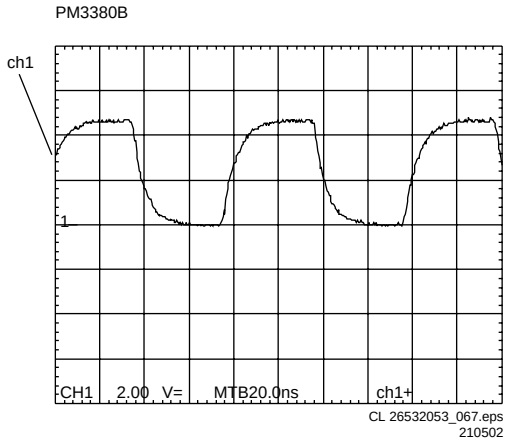


Figure 5-12 PCMCLK

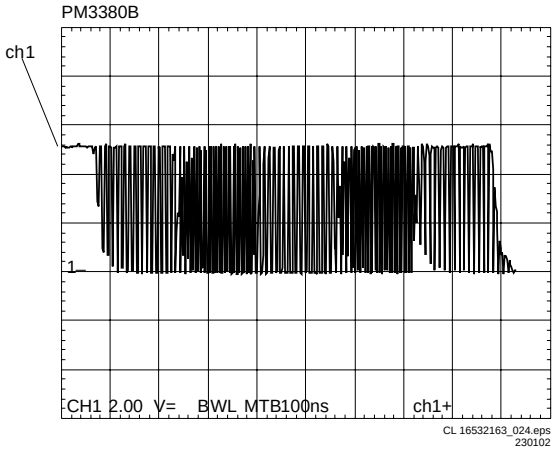


Figure 5-13 SPDIF

To switch the audio signal OFF, press the STOP button on the front.
Without A/V board, the switching levels are as follows:

– DATA_LsRs and DATA_CL switch between low and high for pink noise. For sine, this is low.
– PCMDATA0, PCMLRCLK, PCMCLK and PCMSCLK switches between low and high for both pink noise and sine.
– SPDIF switches between LOW and HIGH

Alternatively, there is a check that can be done without A/V board.
First, let the decoder generate pink noise on the audio outputs.

Table 5-14

Ref. #	Command Name	Remark
20a	AudioPinkNoiseOn	Audio Pinknoise On

Measure then these signals on level and frequency.

Table 5-15

Signal	Level between	Frequency
PCMLRCLK	low/high	48kHz 0.02%
PCMSCLK	low/high	3.072MHz 0.02%
PCMCLK	low/high	12.288MHz 0.02%
PCMDATA	low/high	N/A
SPDIF	LOW/HIGH	N/A

Put the pink noise off:

Table 5-16

Ref. #	Command Name	Remark
20b	AudioPinkNoiseOff	Audio Pinknoise Off

5.5 VIDEO

5.5.1 Video Output Check

Measure the DC voltages at all video-outputs at conn 1703 while the video signal is turned off: 1V ± 10%
Generate a color-bar via next software commands:

Ref. #	Command Name	Remark
23a	VideoColDencOn	Colourbar DENC ON
61a	VideoColOutRGB	RGB Colourbar
61b	VideoColOutYUV	YUV Colourbar
23b	VideoColDencOff	Colourbar DENC OFF

Check video output at the next testpoints:

Name	Testpoint	Waveform
R_VID (V)	F795	Refer to Figure 5-14 5-20
G_VID (Y)	F796	Refer to Figure 5-15
B_VID (U)	F799	Refer to Figure 5-16 5-21
CVBS_VID	F788	Refer to Figure 5-17
C_VID	F791	Refer to Figure 5-18
Y_VID	F792/F796	Refer to Figure 5-19

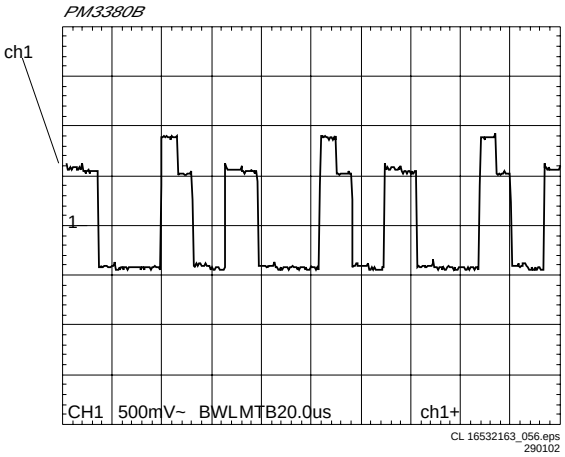


Figure 5-14 R_VID (V) with video out at RGB

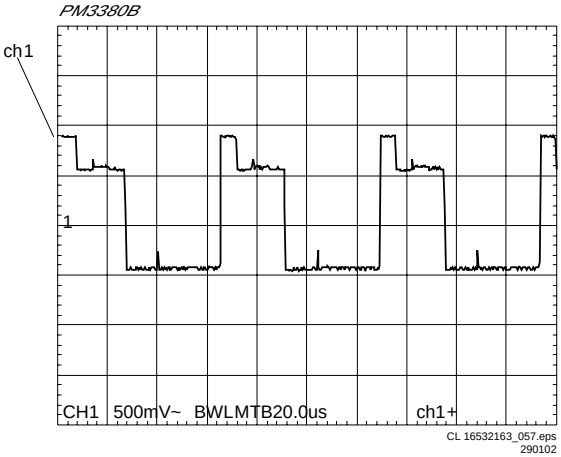


Figure 5-15 G_VID (Y) with video out at RGB

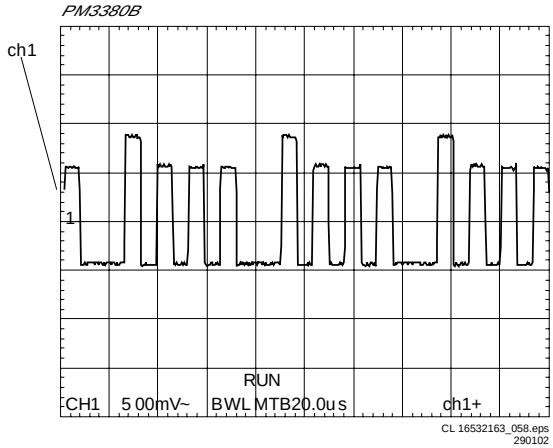


Figure 5-16 B_VID (U) with video out at RGB

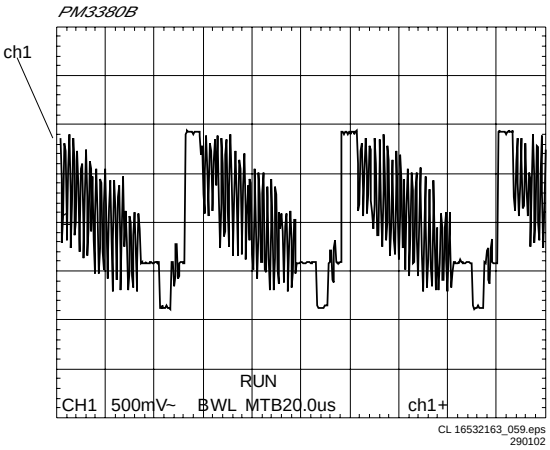


Figure 5-17 CVBS_VID

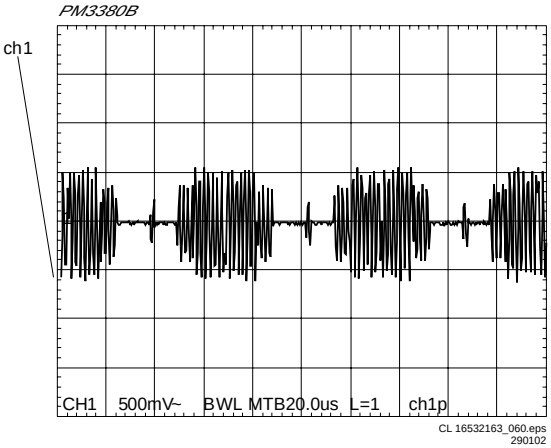


Figure 5-18 C_VID

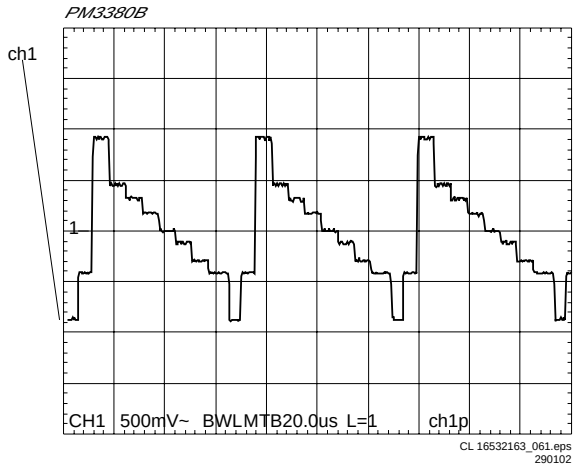


Figure 5-19 Y_VID

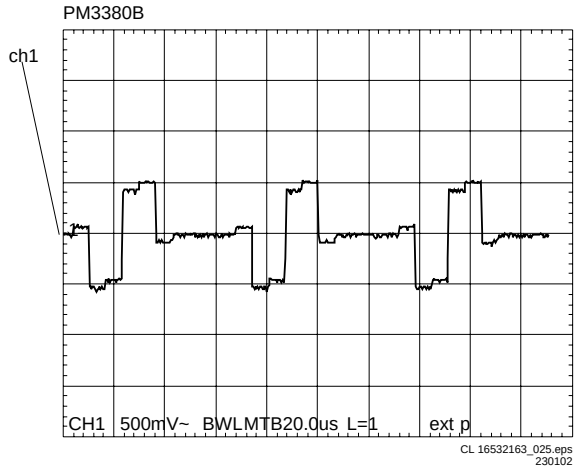


Figure 5-20 R_VID (V) with video out at YUV

5.5.3 Video Hsync Check.

To measure the Video Hsync, the connector 1704 must be connected to the external video processing device such as high quality progressive scan codex and high quality Video DAC, else there will not be any waveform. To check for the Hsync, the following commands can be used:

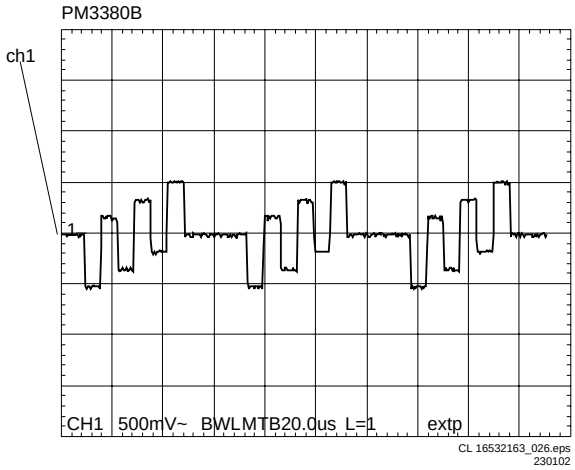


Figure 5-21 B_VID (U) with video out at YUV

5.5.2 Slow Blanking Scart

An aditional part of the video-path is the scart function-switching test. The scart function-switching pin has three levels which depend on the level of the output ports SCART0 and SCART1. These latter two signals are driven by the output pins PIO3.6 and PIO3.7 of the STi55xx.
Check the level of SCART0 and SCART1 with the following commands:

Table 5-17 Slow blanking scart

Ref. #	Command Name	Scart0 (PIO3.6)	Scart1 (PIO3.7)	Level on Pin 8 of scart
25a	VideoScartLo	1	1	0-2V
25b	VideoScartMi	0	1	4.5-7V
25c	VideoScartHi	0	0	9.5-12V

Table 5-18 Video Hsync check

Ref. #	Command Name	Remark	Value	Waveform
23a	VideoColDencOn	ColourbarDENC ON	15.625 kHz 0.02% Vpeak-peak > 3V	Refer to Fig 5-22
61a	VideoColOutRGB	RGB Colourbar ON	15.625 kHz 0.02% Vpeak-peak > 3V	Refer to Fig 5-22
23b	VideoColDencOff	Colourbar DENC OFF	No measurements needed	

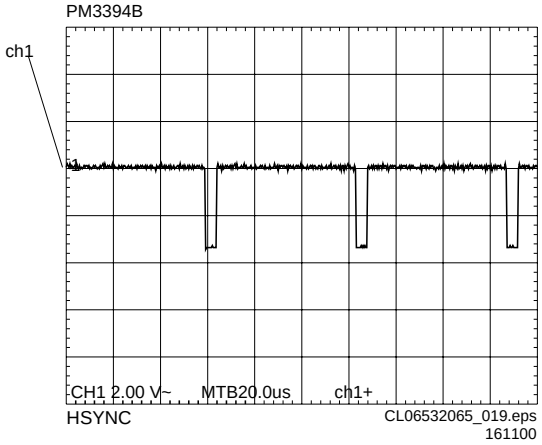


Figure 5-22 Video H Sync

5.6 Servo

5.6.1 General Start-up Measurements:

Reset the Basic Engine part

Table 5-19 Reset basic engine part

Ref. #	Command Name	Remark
44	BeReset	Reset the Basic Engine

Check if the Servo Reset (RSTN) at testpoint F258 goes from low to high after executing BeReset commands.

Check Vref

Table 5-20 Vref check

Name	Testpoint	Value
Vref	F111	2.5V 0.3V

Play DVD test Disc and check I2S interface

Table 5-21 I2S interface check

Name	Testpoint	Value	Value
BE_BCLK	F200	6.0 MHz ± 0.1	Refer to Figure 5-23
BE_WCLK	F201	high	Refer to Figure 5-25
BE_DATA	F202	low	Refer to Figure 5-24
BE_FLAG	F203	low	No waveform
BE_V4	F255	low	No waveform
BE_SYNC	F256	low	No waveform

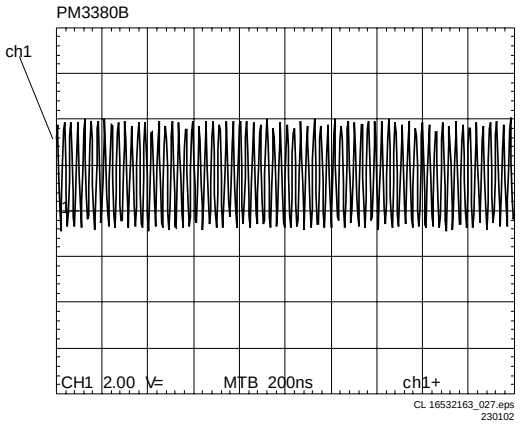


Figure 5-23 BE_BCLK

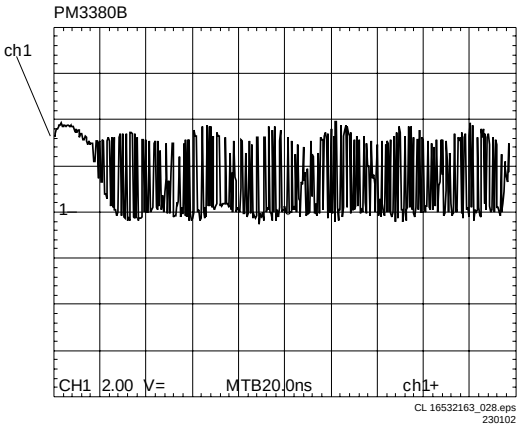


Figure 5-24 BE_DATA

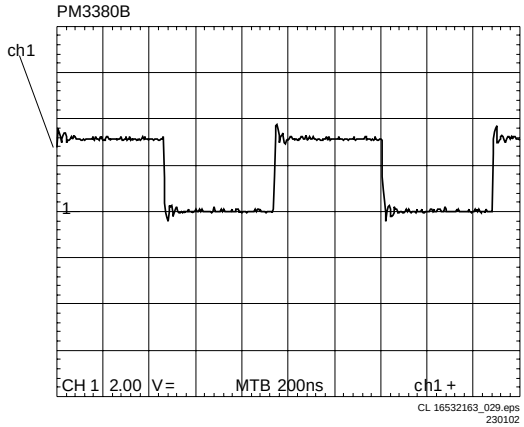


Figure 5-25 BE_WCLK

5.6.2 Spindle Motor:

Before switching on the discmotor, check the following testpoints:

Table 5-22 Spindle motor check

Name	Testpoint	Value
STDBY_MOTOR	F308	low
MOTO1	F350	1V5 0.3

Switch the Discmotor ON/OFF with the following commands:

Table 5-23 Disc motor switching

Ref. #	Command Name	Remark
39a	BeDiscmotorOn	Discmotor on
39b	BeDiscmotorOff	Discmotor off

Check the following signals with the discmotor switched ON and without DVD Disc inserted.

Table 5-24 Disc motor switching

Name	Testpoint	Frequency
STDBY_MOTOR	F308	high
MOTO1	I241	4Vpp ± 0.5V Refer to Figure 5-26
A3	F301	Refer to Figure 5-27
A2	F302	Refer to Figure 5-27
A1	F303	Refer to Figure 5-27
T1	F210	Refer to Figure 5-28
T2	F211	Refer to Figure 5-28
T3	F212	Refer to Figure 5-28
H1+	F306	Refer to Figure 5-29
H1-	F304	Refer to Figure 5-29
H2+	F309	Refer to Figure 5-29
H2-	F305	Refer to Figure 5-29
H3+	F311	Refer to Figure 5-29
H3-	F313	Refer to Figure 5-29

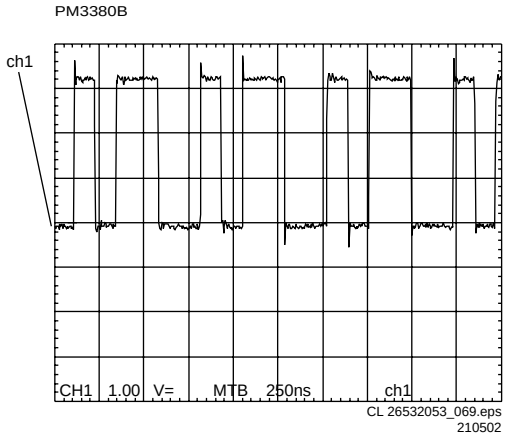


Figure 5-26 Motor 1

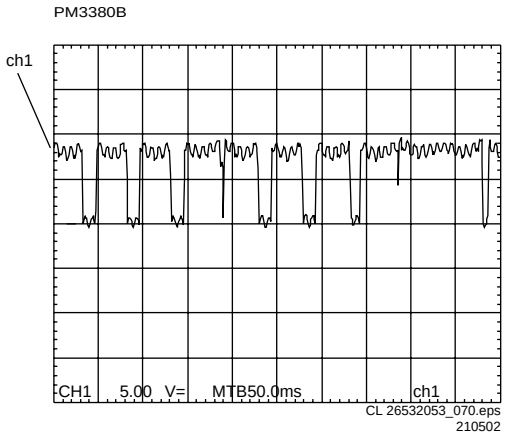


Figure 5-27 A1-A2-A3

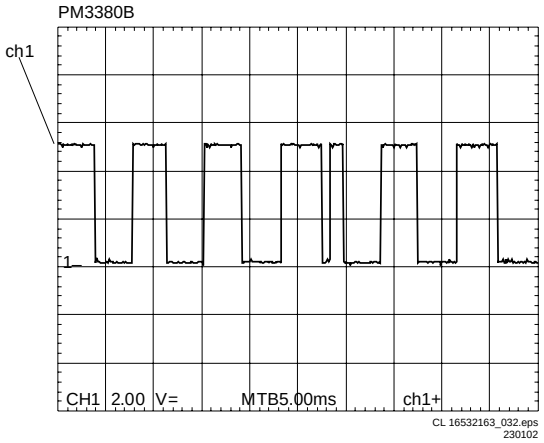


Figure 5-28 T1-T2-T3

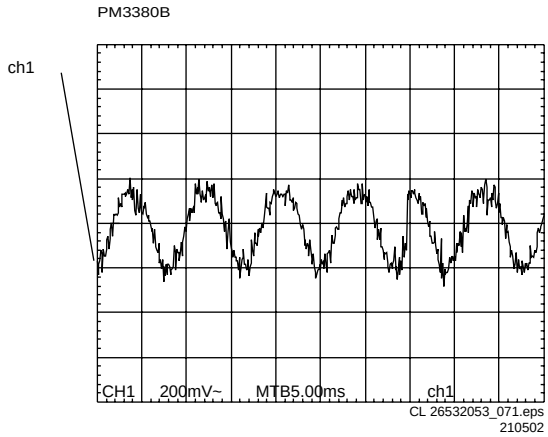


Figure 5-29 H1+ ; H1- ; H2+ ; H2- ; H3+ ; H3-

When measurement is completed, switch the discmotor OFF before executing next command

5.6.3 Radial

Radial ON will only work when the PCB is connected to a CDM and DVD Disc is inserted.
Switch the Radial control ON/OFF with the following commands:

Table 5-25 Radial

Ref. #	Command Name	Remark
40a	BeRadialOn	Radial control on
40b	BeRadialOff	Radial control off

Check the following signals before Radial control ON/OFF

Table 5-26 Radial

Name	Testpoint	Value (Radial ON)
Rad -	F132	4.3V 0.5V
Rad +	F133	4.3V 0.5V
RA	F218	Refer to Figure 5-30 and 5-31

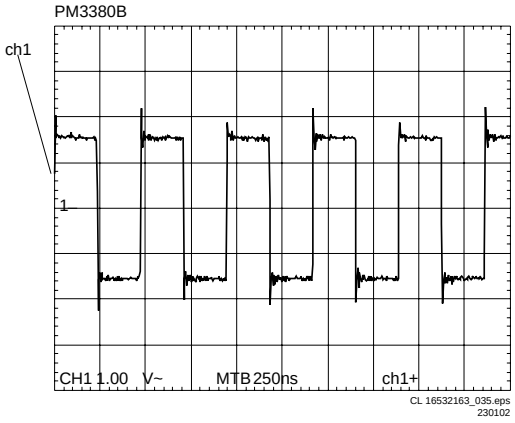


Figure 5-30 RA (BeRadialOff)

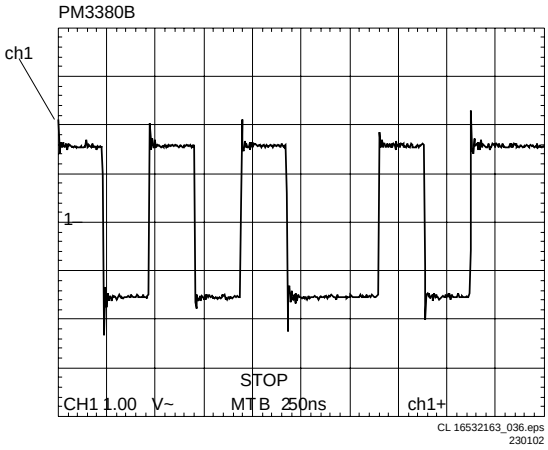


Figure 5-31 RA (BeRadialOn)

Visual check on the laser,when Radial control ON, if the laserlight is visible.
Once the check is completed,switch the Radial control OFF before executing next command

5.6.4 Sledge

Test need a DVD disc in the DVD player to operate properly.
Use the following commands to move the sledge:

Table 5-27 Sledge

Ref. #	Command Name	Remark
41a	BeSledgeIn	Sledge inwards
41b	BeSledgeOut	Sledge outwards

Check for the waveform (Figure 5-32) of SL at testpoint F219

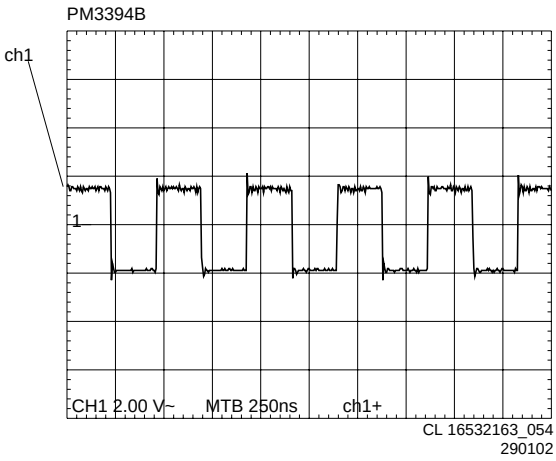


Figure 5-32 SL

Check DC vtg on the following testpoint when Sledge at Inward / Outward position

Table 5-28 DC vtg check

Name	Testpoint	Value
SL -	F327	4.5V 0.5V
SL +	F326	4.5V 0.5V

Measure peak to peak signal on SL- and SL+ while moving sledge outwards.
Signal will only appear momentary during command BeSledgeOut

Table 5-29

Name	Testpoint	Waveform
SL -	F327	Refer to Figure 5-33
SL +	F326	Refer to Figure 5-33

Measure input sledge control (sledge in HOME position)

Table 5-30 Input sledge control

Name	Testpoint	Value
SINPHI	F347	1.5V 0.5V
COSPHI	F346	1.5V 0.5V

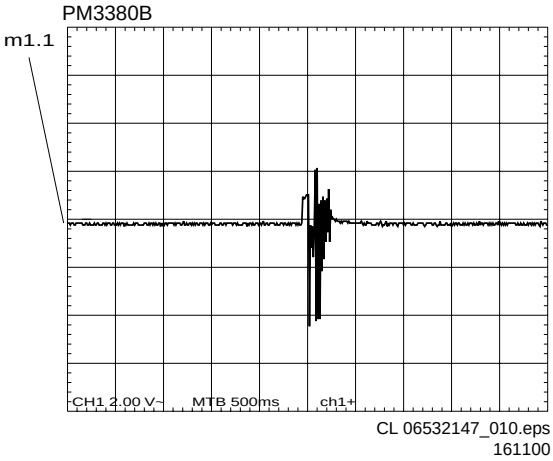


Figure 5-33 SL+ / SL- (SLEDGE OUTWARDS)

5.6.5 Tray:

To open and close the tray use the following commands:

Table 5-31 Tray

Ref. #	Command Name	Remark
43a	BeTrayIn	Tray in
43b	BeTrayOut	Tray out

Measure voltage at the driver outputs of the BA5938FM for the tray closed.

Table 5-32 Tray closes

Name	Testpoint	Value (Tray closed)
TRAY -	F340	4.3V 2.0V
TRAY +	F338	4.3V 2.0V

Measure voltage and waveform at driver outputs while the tray is opening.

Table 5-33 Tray opens

Name	Testpoint	Value (Tray opening)
TRAY -	F340	2.0V 1.0V
TRAY +	F338	6.0V 1.0V

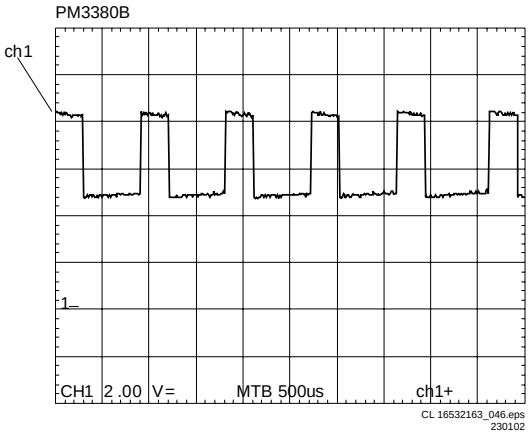


Figure 5-34 TRAY -

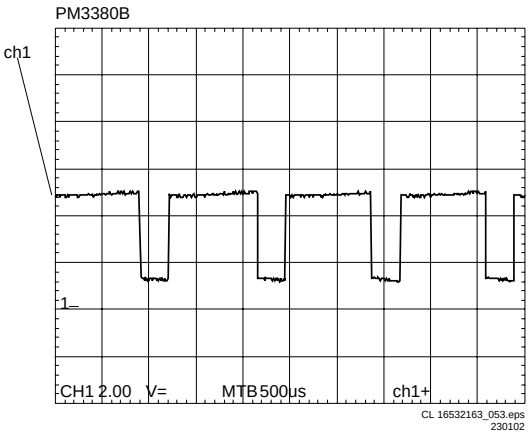


Figure 5-35 TRAY +

5.6.6 Focus

Test need a DVD disc in the DVD player to operate properly.
To switch the Focus motor on/off, use the following commands:

Table 5-34 Focus motor switching

Ref. #	Command Name	Remark
38a	BeFocusOn	Focus on
38b	BefocusOff	Focus off

Measure the driver outputs of the BA5938FM for the Focus OFF.

Table 5-35 Focus motor switching

Name	Testpoint	Value (Focus OFF)
FOC -	F134	5V 0.5V
FOC +	F130	5V 0.5V
FO	F220	1.5V 0.3V

Switch the focus ON and measure again the driver outputs

Table 5-36 Focus motor switching

Name	Testpoint	Value	Waveform
FOC -	F134	1Vpp 0.2V	Refer to Figure 5-36
FOC +	F130	1Vpp 0.2V	Refer to Figure 5-36
FO	F220		Refer to Figure 5-37/38

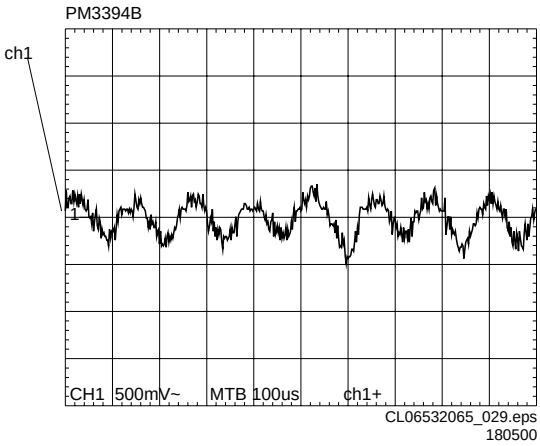


Figure 5-36 FOC+ (BefocusOn)

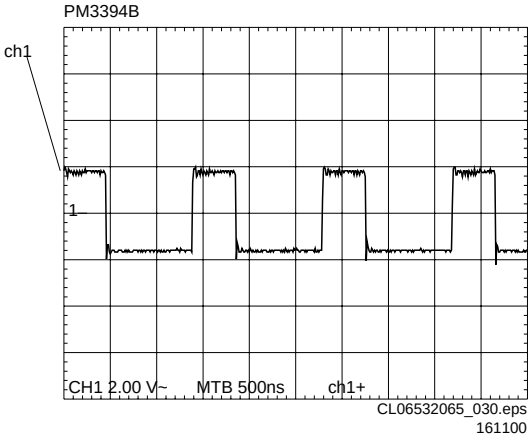


Figure 5-37 FO (BefocusOff)

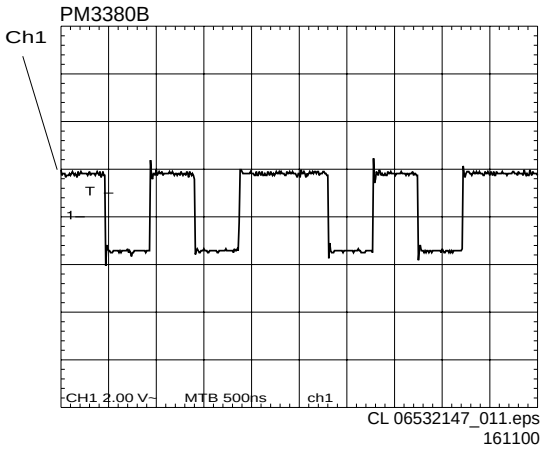


Figure 5-38 FO (BefocusOn)

Visual check on the laser,when Focus control ON, if the laserlight is visible.
Once the check is completed,switch the focus control OFF before executing next command.

5.6.7 Hf Path

Play DVD Test Disc.
Measure outputs of diodes Ax, B, C, D, E, F.

Table 5-37

Name	Testpoint	Value
Ax	F119	2.6V 0.2%
B	F127	2.6V 0.2%
C	F124	2.6V 0.2%
D	F122	2.6V 0.2%
E	F115	2.6V 0.2%
F	F117	2.6V 0.2%

At outputs of diodes A, B, C, D the following waveform can be measured: Refer to Figure 5-39

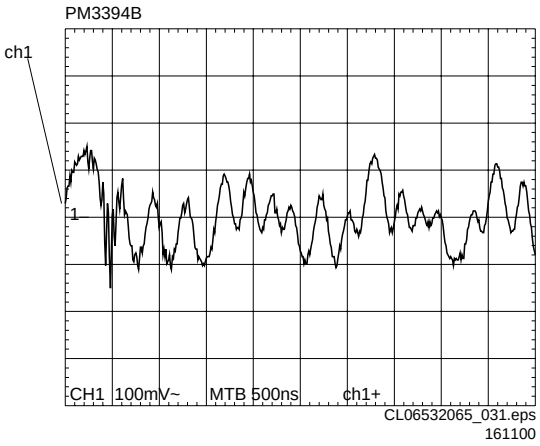


Figure 5-39 Output of diodes A,B,C,D

Measure DVDALAS outputs

Table 5-38 DVDALAS outputs

Name	Testpoint	Value
OA	F104	1V 10%
OB	F107	1V 10%
OC	F108	1V 10%
OD	F110	1V 10%
S1	F113	1V 10%
S2	F112	1V 10%

At output HFN, the following waveform can be measured : Refer to Figure 5-40

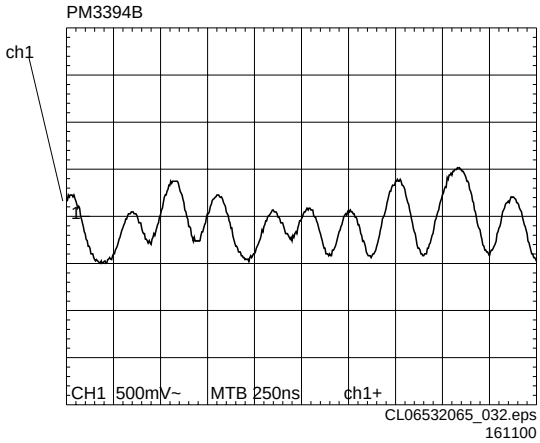


Figure 5-40 HFN / HFP

5.7 Diagnostic Software Description

5.7.1 Introduction

Purpose
This document describes all interfaces from the outside world to the diagnostic software, what is needed to use these interfaces and how to access them.

Scope
This document has been realised within the framework of the DVD video player.

5.7.2 Definitions and Abbreviations

Definitions

Control PC	Automatic test equipment, part of the production control system in the factory, to control the execution of Diagnostic Nuclei in the DVD player.
Diagnostic Nucleus	Part of the Diagnostic Software. Each nucleus contains an atomic and software independent diagnostic test, testing a functional part of the DVD player hardware on component level.
Script	Part of the Diagnostic Software. Each script contains a sequence of Diagnostic Nuclei to be executed.
Service PC	PC used by a service- or repair-person to communicate with the Diagnostic Software in the DVD player.

Abbreviations

FDS	Full Diagnostic Software

5.8 Overview of Interfaces

The table below shows an overview of the user interfaces of the Diagnostic Software. The table is based on logical interface, interfaces as seen from user perspective. A logical interface can use one or more physical interface components. The DVD has only a single RS232 port, implying that all interfaces using this port are mutually exclusive.

Table 5-39 Interface overview

Logical Interface	Description	Physical interface components
Menu Interface	Menu-driven activation of individual nuclei, used for Level 2/ Second Line diagnostic mode. Users are service or repair people	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin
Command Line Interface	Used during Level 1 diagnostic mode. Used to send commands from the Control PC into the DVD hardware.	Control PC, running a control program (e.g. Asterix), connected to RS232 port of the DVD player Test pin
Script Interface	Used to execute Player Test Script (including reading the error log) and Dealer Test Script.	Local keyboard Local display
S2B interface	Used for S2B communication with the Basic Engine	Service PC, running a S2B monitor program, connected to the RS232 port of DVD player Test pin
Download Interface	Used to download diagnostic software into the DVD player	Service PC running a terminal emulation program, connected to the RS232 port of the DVD player Test pin

- In the next chapters the logical user interfaces are described in more detail including the exact use of the physical interface components.
- **Front Panel Key Usage:**
  Some of the nuclei used in the diagnostic software require user intervention through the front panel key.

5.9 Description of Interfaces

5.9.1 Menu Interface

The menu interface is part of the Level 2 / Second Line diagnostic mode. Via the menu interface it is possible to control the execution of the Diagnostic Nuclei.

Set-up Physical Interface Components
Hardware required:
- Service PC
- one free COM port on the Service PC
- special cable to connect DVD player to Service PC

The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm /Windows Hyperterminal) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM port must be connected via a special cable to the RS232 port of the DVD player. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin).

Activation
Switch the player on and the following text will appear on the screen of the terminal (program):

```
DVDv4 Diagnostic Software version 5.03

(M)enu, (C)ommand or (S)2B interface ? [M]:@ m <enter>

SDRAM Interconnection test passed
Basic SDRAM test passed
Slave Processor: SLAVE2

Press ENTER to go to Main Menu
CC: >                                          CL 26532053_045.eps
                                                          130502
```

Figure 5-41

1. The first line indicates that the Diagnostic software has been activated and contains the version number of the diagnostic; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully.
2. The second line is the prompt asking the user to choose the interface format. Enter ‘M’ to select Menu mode and the next three lines are the successful result of the two subsequent basic tests (nuclei 2, 4 and the detection of the display type used by the panel respectively).
3. The third line indicates the results ofthe shared SDRAM interconnection test.
4. The fourth line indicates the results of tyhe shared SDRAM read/write test.
5. The fifth line indicates what front panel processor was connected to the monoboard. It could be one of the following: SLAVE2, SLAVE3, SLAVE 4, or Not Detected.
6. The last line is the prompt (‘CC>’). Press ‘ENTER’ key and the main menu will appear. For the layout of the menus, see chapter ‘Layout of Menu and Submenu’

To switch between interfaces, the DVD player needs to be switched off and on again.

Note: For player that has no Mechanical power switch, it can be turned on by connecting the power-cable.

Usage
To select, type the number of the chosen menu-item at the prompt. Each entry must be terminated with a ‘RETURN’. Invalid selections will cause an error message by the Menu Handler
Example:

```
Select > 99
Invalid menu choice, number out of range ER @
Press RETURN to continue … @
                                               CL 16532163_038.eps
                                                          230102
```

Result and output of an activated (and terminated) nucleus will be sent back to the service terminal. **Example:**

```
Select > 3
1601 Data line X is not connected to the SDRAM ER @
Press RETURN to continue … @
                                               CL 16532163_039.eps
                                                          230102
```

After the user presses a key, the current menu is rebuilt on screen.
Pressing “RETURN” at the prompt without any further input at the terminal will always rebuild the main menu.

Termination
The menu interface is terminated by switching off the DVD player.

5.9.2 Command Line Interface

The command line interface is part of level 1 diagnostic mode. Via a command line interface the execution of Diagnostic Nuclei can be controlled.

Set-up Physical Interface Components
Hardware required:
- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to the Control PC

The control PC must use the following port settings for the used COM port: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The control PC is connected with a special cable to the RS232 port of the DVD player. Via the same connection the test pin will be connected to ground.

Activation
After power on the next text will sent to the control PC

```
DVDv4 Diagnostic Software version 5.03

(M)enu, (C)ommand, or (S)2B interface ? [M]:@ C <enter>

SDRAM Interconnection test passed
Basic SDRAM test passed
Front Panel Processor: SLAVE2

DD: >
```

CL 26532053_073.eps
220502

The first line indicates that the Diagnostic software has been activated and contains the version number; this is also an indication that the first basic nucleus (nucleus number 1) has been executed succesfully. The second line lets the user choose the interface format. Enter 'C' to select Command Mode and the next three lines are the succesful result of the two subsequent basic tests (nuclei 2, 4 and the detection of the display type used by the panel respectively). If not all these messages appear on the terminal screen, then the related nucleus found an error. The last line is the prompt ("DD>"). The diagnostic software is now ready to receive commands.

Note: For player that has no Mechanical power switch, it can be turned on by connecting the power-cable.

Usage
The commands that can be given are the numbers of the nuclei. A command must be terminated with a <RETURN> character from the control PC. When typing commands, the backspace key can be used to make corrections.
In case of typing errors in the command, an error message is returned. **Example:**

```
DD: > CompSdarmWrR?       (Nuclei name cannot be accepted)
0001 Unknown command ER @
DD: >
```

CL 16532163_041.eps
230102

If the command (the nucleus number) is recognised, the nucleus is executed. Result and output of an activated (and terminated) nucleus will be sent back to the control PC according to the standard layout.

Example for a command without error:

```
DD: > 16        (Execute CompSdramWrR nuclei)
1600 OK @
DD: >
```

CL 16532163_042.eps
230102

Example for a command with error:

```
DD: > 16
1601 Address line X not connected to the SDRAM @
DD: >
```

CL 16532163_043.eps
230102

Termination
The command line interface is terminated by switching off the DVD player.

5.9.3 S2B Interface

Set-up Physical Interface Components
Hardware needed:
- Control PC
- one free COM port on the Control PC
- special cable to connect DVD player to Control PC
- S2B monitor tool running on the Control PC

Activation
To start the S2B interface, connect the RS232 cable to the Control PC in the correct manner. Then start the PC, start the monitor tool and start the DVD player; turn off the monitor tool, turn on S2B monitor tool. The S2B monitor tool now takes all communication.
The S2B interface is activated by sending the bit pattern 110x xxxx with the first character to the DVD player, when the user is asked to choose an interface type. The command handler will then activate the S2B pass-through nucleus. The character sent will be passed to this nucleus without loss.

Note: For player that has no Mechanical power switch, it can be turned on by connecting the power-cable.

Termination
To terminate S2B pass-through mode, switch off the DVD player.

5.10 Script Interfaces

This interface is used during execution of the Player Script and the Dealer Script to display output and error messages on the local display of the stand-alone DVD player.

The activation and the usage can refer to the respective stand-alone DVD player service manual

5.10.1 Layout of Menu and Submenu

Layout Of Menus And Submenus For The Service Terminal
NOTE: a symbol "--" in the menu layouts indicates that that specific menu choice will invoke the display of a submenu. This symbol will also be used in the implementation of the menus (i.e. the "--" will also appear in the user interface).

Menus

MAIN MENU
1 Audio...
2 Video...

3 Front Panel...
4 Basic Engine...
5 Processor Peripherals...
6 Error Log...
7 Furore...
8 Miscellaneous...

First Level Submenus

MAIN > AUDIO MENU
1 Mute...
2 Pink Noise...
3 Sine Wave...
4 Digital Ports...
5 Ext. DAC Board...

MAIN > VIDEO MENU
1 Colourbar...
2 Scart...
3 Digital Port...

MAIN > FRONT PANEL MENU
1 Slave Processor...
2 VFT Display [30a]
3 LCD Display [30b]
4 LCD BkLight [30c]
5 Keyboard [27]
6 LEDs [29]
7 Remote Control [28]
8 P50 Check [60]

MAIN > BASIC ENGINE MENU
1 Reset [44]
2 Version [37]
3 S2B...
4 Loader Mechanism...
5 Special Diagnostics...

MAIN > PROCESSOR PERIPHERALS MENU
1 Clock...
2 Flash...
3 NVRAM...
4 SDRAM Write/Read [16]

MAIN > ERROR LOG MENU
1 Read Last Errors [31]
2 Read Error Bits [32]
3 Reset Error Log [33]

MAIN > FURORE MENU
1 SDRAM Write/Read [63]
2 SDRAM Write/Read [64]
3 Chip Revision ID [65]
3 Set Output High [84a]
3 Set Output Low [84b]
3 Reset [83]

MAIN > MISCELLANEOUS MENU
1 Statistics Info...
2 Read DVD Application version [46]

Second Level Submenus

MAIN > AUDIO > MUTE MENU
1 Mute On [19a]
2 Mute Off [19b]

MAIN > AUDIO > PINK NOISE MENU
1 Pink Noise On [20a]
2 Pink Noise / Beep Tone Off [20b]
3 Beep Tone On [20c]

MAIN > AUDIO > SINE WAVE MENU
1 Audio Sine On [21a]
2 Audio Burst On [21b]

MAIN > AUDIO > DIGITAL PORTS MENU
1 LFE_SEL High [56a]
2 LFE_SEL Low [56b]

MAIN > AUDIO > EXT DAC BOARD MENU
1. DAC Reset [79]
2. I2C Test...
3. Clock...
4. Audio...
5. Low Power Standby...
6. DAC Mode...

MAIN > VIDEO > COLOURBAR MENU
1 Colourbar DENC On (PAL) [23a]
2 Colourbar DENC On (NTSC) [23c]
3 Colourbar DENC/MPEG Off [23b]
4 ProgressiveScan MPEG On [24a]
5 Enhanced YUV MPEG On [24b]
6 Set Video Out To RGB [61a]
7 Set Video Out To YUV [61b]

MAIN > VIDEO > SCART MENU
1 I2C Scart IC Check [54]
2 Scart To DVD [55a]
3 Scart Pass Through [55b]
4 Scart Pin 8 Low (0 to 2)V [25a]
5 Scart Pin 8 Mid (4.5 to 7)V [25b]
6 Scart Pin 8 Hi(9.5 to 12)V [25c]

MAIN > VIDEO > DIGITAL PORT MENU
1 Video Port Out 0xAA [17a]
2 Video Port Out 0x55 [17b]

MAIN > FRONT PANEL > SLAVE PROCESSOR MENU
1 Bus Comms Check [12]
2 S/W Version [26]

MAIN > BASIC ENGINE > S2B MENU
1 S2B Echo [13]
2 S2B Pass-Through [14]

MAIN > BASIC ENGINE > MECHANISM MENU
1 Disc Motor...
2 Laser...
3 Tray...
4 Focus...
5 Radial...
6 Sledge...
7 Grooves...

MAIN > BASIC ENGINE > SPECIAL DIAGNOSTICS MENU
1 Read FlashID [70]
2 ROM Checksum [71]
3 Scratch Detector Test [72]

MAIN > PROCESSOR PERIPHERALS > PCM CLOCK MENU
1 PCM_CLK In CDDA Mode (11.3MHz) [8a]
2 PCM_CLK In DVD Mode (12.3MHz) [8b]
3 PCM_CLK In DVD96kHz Mode (24.6MHz) [8c]

MAIN > PROCESSOR PERIPHERALS > FLASH MENU
1 Verify FLASH Checksum [6]
2 Show FLASH Checksum [62]

MAIN > PROCESSOR PERIPHERALS > NVRAM MENU
1 I2C NVRAM Acces [11]
2 NVRAM Config [34]
3 NVRAM Reset [35]

4 NVRAM Modify [36]
5 NVRAM Read/Wr Test [15]

MAIN > MISCELLANEOUS > STATISTICS INFO MENU
1 Total Nr Of Times Tray Open [47a]
2 Total Time Power On [47b]
3 Total Play-Time CDDA & VCD [47c]
4 Total Play-Time DVD [47d]

Third Level Submenus

MAIN > AUDIO > EXT DAC BOARD > I2C TEST MENU
1. I2C Test [66a]
2. I2C Enable Pin On [66b]
3. I2C Enable Pin Off [66c]

MAIN > AUDIO > EXT DAC BOARD > CLOCK MENU
1. Clock Internal [67a]
2. Clock External [67b]
3. Clock Upsampling 192k (963 only) [82a]
4. Clock Upsampling 96k (963 only) [82b]
5. Clock Upsampling On (963 only) [82c]
6. Clock Upsampling Off (963 only) [82d]

MAIN > AUDIO > EXT DAC BOARD > AUDIO
1. Audio Pre-Mute On [68a]
2. Audio Pre-Mute Off [68b]
3. Audio Center On [69a]
4. Audio Center Off [69b]

MAIN > AUDIO > EXT DAC BOARD > LOW POWER STANDBY
1. Low Power Standby On [81a]
2. Low Power Standby Off [81b]

MAIN > AUDIO > EXT DAC BOARD > DAC MODE MENU
1. DAC CDDA Mode [80a]
2. DAC DVD48 Mode [80b]
3. DAC DVD96 Mode [80c]
4. DAC DSD Mode [80d

MAIN > BASIC ENGINE > MECHANISM > DISC MOTOR MENU
1 Disc Motor On [39a]
2 Disc Motor Off [39b]

MAIN > BASIC ENGINE > MECHANISM > LASER MENU
1 CD Laser On [58a]
2 CD Laser Off [58b]
3 DVD Laser On [58c]
4 DVD Laser Off [58d]

MAIN > BASIC ENGINE > MECHANISM > TRAY MENU
1 Tray Open [43b]
2 Tray Close [43a]

MAIN > BASIC ENGINE > MECHANISM > FOCUS MENU
1 Focus On [38a] (load DVD first)
2 Focus Off [38b]

MAIN > BASIC ENGINE > MECHANISM > RADIAL MENU
1 Radial Control On [40a] (load DVD first)
2 Radial Control Off [40b]

MAIN > BASIC ENGINE > MECHANISM > SLEDGE MENU
1 Sledge Inwards [41a]
2 Sledge Outwards [41b]

MAIN > BASIC ENGINE > MECHANISM > GROOVES (Uses DVD) MENU
1 Jump To Inside Grooves [42a]
2 Jump To Middle Grooves [42b]
3 Jump To Outside Grooves [42c]

Screen Layout With Menus
When menus are used, no specific screen layout can be given: menu information will not be in a special format, except for the layout as mentioned in the previous paragraphs.

A typical menu session can look as follows:

```
DVDv4 Diagnostic Software version 5.03


(M)enu, (C)ommand or (S)2B interface ? [M]:@ <enter>
SDRAM Interconnection test passed
Basic SDRAM test passed
Slave Processor: SLAVE2


Press ENTER to go to main menu
CC: > <enter>

MAIN MENU

1. Audio ...
2. Video ...
3. Front Panel ...
4. Basic Engine ...
5. Processor Peripherals ...
7. Furore ...
8. Miscellaneous ...

Select > 4 <enter>

MAIN > BASIC ENGINE MENU

1. Reset [44]
2. Version [37]
3. S2B
4. Loader Mechanism ...
5. Special Diagnostics ...

Press Enter to go to Main Menu

Select > 5 <enter>

MAIN > BASIC ENGINE > SPECIAL DIAGNOSTIC MENU

1. Read flashID [70]
2. ROM checksum [71]
3. Scratsh detector test [72]
Press Enter to go to Main Menu
```

CL 26532053_047.eps 240502

Figure 5-42

Depending on the height of the screen, the text will start scrolling off the top of the screen.

Layout Of Results Diagnostic Nuclei On Control/service Pc
Results returned from a Diagnostic Nucleus to the control/ service PC will have a maximum length of 300 characters and are terminated by a CR character (included in the string length) The result has the following layout
< number >< string > [OK l ER] @< CR >
The use of the "@" enables the Asterix system on the Control PC to parse the output string of each nucleus into a database.

< number > is a 4-digit decimal number padded with leading zeros if its value is less than 4 digits. The first two digits identify the generating nucleus (or goup of nuclei), the latter two digits indicate the error number.

< string > is a text string containing information about the result of the Diagnostic Nucleus.

< number > and < string > are defined in [SDD_DN] in the output sections of each Nucleus.
Examples:

```
1. 0001 Unknown command ER @
2. 3100 OK @
3. 0901 Data line X is not connected to the DRAM ER @
4. Device ID: 0x01
Manufac ID: 0xC2
7000 OK @
```

CL 16532163_045.eps 230102

5.11 Diagnostic Nuclei

Each nucleus contains an atomic and independent diagnostic test, testing a functional part of the DVD player hardware on component level. Each Nucleus returns a result message to its caller. Some tests (e.g. generating a colour bar) can only return an "OK" result. Internal communication will be done via a uniform interface between the diagnostic Engine, Scripts and the Diagnostic Nuclei.
The diagnostic Engine can only operate if a certain (minimal) set of hardware is functioning properly. To test this set of hardware, a set of basic diagnostic nuclei is embedded in the DVD player. Each basic diagnostic nucleus will only test that part of the hardware which is required for execution of the diagnostic Engine, e.g. a RAM test will only test that part of RAM that is used by the diagnostic engine. After the Diagnostic Engine is operational it is possible to do a full RAM diagnostic. All basic diagnostic nuclei start with prefix 'Basic'.
In the overview each Diagnostic Nucleus consists of a reference number, a reference name and remarks. Reference number and name are coupled and one of them is enough for unique identification.

Table 5-40 Basic diagnostic nuclei

Ref. #	Reference Name	Remark
1	BasicSpAcc	Serial port Access test/ initialization
2a	BasicInterconDram	Data and address bus Interconnection (only for development)
2b	BasicInterconSdram	Data and address bus interconnection
3	BasicDramWrR	DRAM Write Read (only for development)
4	BasicSdramWrR	SDRAM Write Read

Table 5-41 Processor and peripherals

Ref. #	Reference Name	Remark
6	PapChksFl	Checksum FLASH
7a	PapUclkAclkCdda	uClock A_CLK in CD-DA mode
7b	PapUclkAclkDvd	uClock A_CLK in DVD mode
7c	PapUclkAclkDvd96	uClock A_CLK in DVD (96kHz) mode
10	PapFlashWrAcc	FLASH Write Access (only for development)
11	PapI2cNvram	I2C NVRAM access
12	PapI2cDisp	I2C Display PWB
13	PapS2bEcho	S2B Echo
14	PapS2bPass	S2B Pass-through
15	PapNvramWrR	NVRAM Write Read
62	PapChksSum	Show checksums stored in flash

Table 5-42 Components

Ref. #	Reference Name	Remark
16	CompSdramWrR	SDRAM Write Read

Table 5-43 Audio

Ref. #	Reference Name	Remark
19a	AudioMuteOn	Audio Mute On
19b	AudioMuteOff	Audio Mute Off
20a	AudioPinkNoiseOn	Audio Pinknoise On
20b	AudioPinkNoiseOff	Audio Pinknoise (or beep tone) Off
20c	AudioBeepToneOn	Audio Beep Tone On
21a	AudioSineOn	Audio Sine signal On/Off
21b	AudioSineBurst	Audio Sine signal Burst
56a	AudioLfePortHigh	Set the LFE_SEL port to HIGH
56b	AudioLfePortLow	Set the LFE_SEL port to LOW
65	DAC_I2C	Resets DAC and check I2C communication with DAC
66a	DAC_I2CEnable	Enable I2C communication to AV board
66b	DAC_I2CDisable	Disable I2C communication to AV board
67a	DAC_ClockInternal	Uses internal clock from monoboard for DAC (256fs)
67b	DAC_ClockExternal	Uses external clock for DAC (384fs)
68a	DAC_AudioPreMuteOn	Enable Audio Pre-mute pin
68b	DAC_AudioPreMuteOff	Disable Audio Pre-mute pin
69a	DAC_CenterOn	Enable Center on pin
69b	DAC_CenterOff	Disable Center on pin
79	DAC_Reset	Resets DAC
80a	DAC_ModeCDDA	Sets DAC to CDDA mode
80b	DAC_ModeDVD48	Sets DAC to DVD mode (48kHz)
80c	DAC_ModeDVD96	Sets DAC to DVD mode (96kHz)
80d	DAC_ModeDSD	Sets DAC to DSD mode
81a	DAC_LowPowerStandbyOn	Enable Low Power Standby
81b	DAC_LowPowerStandbyOff	Disable Low Power Standby
82a	DAC_UpsamplingFreq192k	Sets Upsampling frequency to 192kHz
82b	DAC_UpsamplingFreq96k	Sets Upsampling frequency to 96kHz
82c	DAC_UpsamplingOn	Enable upsampling
82d	DAC_UpsamplingOff	Disable upsampling

Table 5-44 Video

Ref. #	Reference Name	Remark
17a	VidPortOutAA	Output the value 0XAA at the Digital Video Interface Port
17b	VidPortOut55	Output the value 0X55 at the Digital Video Interface Port
23a	VideoColDencOnPAL	Colourbar (PAL) DENC On
23b	VideoColDencOff	Colourbar DENC Off
23c	VideoColDencOnNTSC	Colourbar (NTSC) DENC On
24a	VideoProgMPEGon	Progressive - DigitalVideo Colour Bar ON
24b	VideoYuvMPEGon	Enhanced YUV-DigitalVideo Colour Bar
25a	VideoScartLo	Scart Low
25b	VideoScartMi	Scart Medium
25c	VideoScartHi	Scart High
54	VideoScartSwComm	Scart Switch communication
55a	VideoScartSwDvd	Scart Switch Dvd
55b	VideoScartSwPass	Scart Switch Pass-through
57a	VideoScartPinLo	PIO-pins as used in 2A for Scart-switching
57b	VideoScartPinMi	PIO-pins as used in 2A for Scart-switching
57c	VideoScartPinHi	PIO-pins as used in 2A for Scart-switching
61a	VideoColOutRGB (ST5508)	Output RGB from ST5508
61b	VideoColOutYUV (ST5508)	Output YUV from ST5508

Table 5-45 Display (slave processor)

Ref. #	Reference Name	Remark
26	DispVer	Version number
27	DispKeyb	Keyboard
28	DispRc	Remote Control
29	DispLed	LEDs
30a	DispDisplay	VFT Display test
30b	DispLCDisplay	LCD Display test
30c	DispLCDBkLight	LCD Backlight test
60	DispP50	P50 loopback test

Table 5-46 Log (Error logging in Nvram)

Ref. #	Reference Name	Remark
31	LogReadErr	Read last Errors
32	LogReadBits	Read errors Bits
33	LogReset	Reset

Table 5-47 Miscellaneous

Ref. #	Reference Name	Remark
34	MiscReadConfig	Read Configuration area from NVRAM
35	MiscNvramReset	NVRAM Reset
36	MiscNvramMod	Modify NVRAM contents
46	MiscApplVer	Read version of application software
47a	MiscTrayOpenNr	Read the number of times the tray opened
47b	MiscPowerOnTime	Read the total time the player's power has been on
47c	MiscPlayTimeCddaVcd	Read the Playtime of CDDA and VCD discs
47d	MiscPlayTimeDvd	Read the Playtime of DVD discs

Table 5-48 Basic engine

Ref. #	Reference Name	Remark
37	BeVer	Version number
38a	BeFocusOn	Focus On
38b	BeFocusOff	Focus Off
39a	BeDiscmotorOn	Discmotor On
39b	BeDiscmotorOff	Discmotor Off
40a	BeRadialOn	Radial control On
40b	BeRadialOff	Radial control Off
41a	BeSledgeIn	Sledge Inwards
41b	BeSledgeOut	Sledge Outwards
42a	BeGroovesIn	jump Grooves to Inside
42b	BeGroovesMid	jump Grooves to Middle
42c	BeGroovesOut	jump Grooves to Outside
43a	BeTrayIn	Tray In
43b	BeTrayOut	Tray Out
44	BeReset	Reset Basic Engine
58a	LaserCdOn	CD Laser on
58b	LaserCdOff	CD Laser off
58c	LaserDvdOn	DVD Laser on
58d	LaserDvdOff	DVD Laser off
70	BedReadFlashID	Read flash memory manufacturer and device ID
71	BedCalcRomChksum	Calculate ROM checksum
72	BedScratchTest	Test scratch detection circuit

Table 5-49 Furore IC

Ref. #	Reference Name	Remark
62	Furore_SdramWrR	Furore SDRAM Write Read test
63	Furore_SdramWrR Fast	Furore SDRAM interconnection test
64	Furore_Id	Furore version ID check
83	Furore_Reset	Furore reset
84a	Furore_High	Sets Furore output pins DSD_PCM0-9 to high
84b	Furore_Low	Sets Furore output pins DSD_PCM0-9 to low

Table 5-50 Karaoke (not available)

Ref. #	Reference Name	Remark
48a	KaraokeModeOff	Switch Karaoke mode off
48b	KaraokeModeOn	Switch Karaoke mode on
49	KaraokeMicInput	Check path from the microphone input to audio output
50a	KaraokeKeyOn	Set Karaoke Key to the maximum level (1200 cent)
50b	KaraokeKeyOff	Set Karaoke Key to flat octave (0 cent)
51a	KaraokeEchoOn	Set Echo Control fuction on
51b	KaraokeEchoOff	Set Echo Control function off

5.12 Nuclei Error Codes

In the following tables the error description of the error codes will be described.

5.12.1 Audio Nuclei

Error code	Error text
1880	Test successful
1800	Test successful
1900	Test successful
1920	Test successful
2000	Test successful
2020	Test successful
2100	Test successful
5600	Test successful
5620	Test successful
7900	"Checksums = 0xA1, 0xB1, 0xC1, 0xD1"
7901	"DAC I2C bus busy"
7902	"DAC I2C expander "
8000	"Test successful"
8001	"DAC mode CDDA I2C bus busy before start"
8002	"DAC mode CDDA I2C connection failed"
8020	"Test successful"
8021	"DAC mode DVD48 I2C bus busy before start"
8022	"DAC mode DVD48 I2C connection failed"
8040	"Test successful"
8041	"DAC mode DVD96 I2C bus busy before start"
8042	"DAC mode DVD96 I2C connection failed"
8060	"Test successful"
8061	"DAC mode DSD I2C bus busy before start"
8062	"DAC mode DSD I2C connection failed"
8100	"Test successful"
8101	"Low Power Standby On I2C bus busy"
8102	"Low Power Standby On I2C connection failed"
8120	"Test successful"
8121	"Low Power Standby Off I2C bus busy"
8122	"Low Power Standby Off I2C connection failed"
8200	"Test successful"
8201	"DAC Upsample 192k I2C bus busy"
8202	"DAC Upsample 192k I2C connection failed"
8220	"Test successful"
8221	"DAC Upsample 96k I2C bus busy"
8222	"DAC Upsample 96k I2C connection failed"
8200	"Test successful"
8201	"DAC UpSample On bus busy"
8202	"DAC UpSample On I2C connection failed"
8200	"Test successful"
8201	"DAC UpSample Off bus busy"
8202	"DAC UpSample Off I2C connection failed"

5.12.2 Basic Engine Nuclei

Error code	Error text
3900	Test successful
3901	“Parity error from Basic Engine to Serial”
3902	“Unexpected response from Basic Engine”
3903	“Communication time-out error”
3904	“Basic Engine returned error number 0xXX”
3921	“Parity error from Basic Engine to Serial”
3922	“Unexpected response from Basic Engine”
3923	“Communication time-out error”
3924	“Basic Engine returned error number 0xXX”
3800	Test successful
3801	“Parity error from Basic Engine to Serial”
3802	“Unexpected response from Basic Engine”
3803	“Communication time-out error”
3804	“Basic Engine returned error number 0xXX”
3805	“Focus loop could not be closed”
3820	Test successful
3821	“Parity error from Basic Engine to Serial”
3822	“Unexpected response from Basic Engine”
3823	“Communication time-out error”
3824	“Basic Engine returned error number 0xXX”
4200	Test successful
4201	“Parity error from Basic Engine to Serial”
4202	“Unexpected response from Basic Engine”
4203	“Communication time-out error”
4204	“Basic Engine returned error number 0xXX”
4205	“Sledge could not be moved to home position”
4206	“Focus loop could not be closed”
4207	“Motor not on speed within time-out”
4208	“Radial loop could not be closed”
4209	“PLL could not lock in accessing or tracking state”
4210	“Subcode or sector information could not be read”
4211	“Requested subcode item could not be found”
4212	“TOC could not be read in time”
4213	“Seek could not be performed”
4220	Test successful
4221	“Parity error from Basic Engine to Serial”
4222	“Unexpected response from Basic Engine”
4223	“Communication time-out error”
4224	“Basic Engine returned error number 0xXX”
4225	“Sledge could not be moved to home position”
4226	“Focus loop could not be closed”
4227	“Motor not on speed within time-out”
4228	“Radial loop could not be closed”
4229	“PLL could not lock in accessing or tracking state”
4230	“Subcode or sector information could not be read”
4231	“Requested subcode item could not be found”
4232	“TOC could not be read in time”
4233	“Seek could not be performed”
4240	Test successful
4241	“Parity error from Basic Engine to Serial”
4242	“Unexpected response from Basic Engine”
4243	“Communication time-out error”
4244	“Basic Engine returned error number 0xXX”
4245	“Sledge could not be moved to home position”
4246	“Focus loop could not be closed”
4247	“Motor not on speed within time-out”
4248	“Radial loop could not be closed”
4249	“PLL could not lock in accessing or tracking state”
4250	“Subcode or sector information could not be read”
4251	“Requested subcode item could not be found”
4252	“TOC could not be read in time”
4253	“Seek could not be performed”
4000	Test successful
4001	“Parity error from Basic Engine to Serial”
4002	“Unexpected response from Basic Engine”
4003	“Communication time-out error”
4004	“Basic Engine returned error number 0xXX”
4005	“Radial loop could not be closed”
4020	Test successful
4021	“Parity error from Basic Engine to Serial”
4022	“Unexpected response from Basic Engine”
4023	“Communication time-out error”
4024	“Basic Engine returned error number 0xXX”
4400	Test successful
4401	Test successful
4100	Test successful
4101	“Parity error from Basic Engine to Serial”
4102	“Unexpected response from Basic Engine”
4103	“Communication time-out error”
4104	“Basic Engine returned error number XX”
4120	Test successful
4121	“Parity error from Basic Engine to Serial”
4122	“Unexpected response from Basic Engine”
4123	“Communication time-out error”
4124	“Basic Engine returned error number XX”
4300	Test successful
4301	“Parity error from Basic Engine to Serial”
4302	“Unexpected response from Basic Engine”
4303	“Communication time-out error”
4304	“Basic Engine returned error number 0xXX”
4320	Test successful
4321	“Parity error from Basic Engine to Serial”
4322	“Unexpected response from Basic Engine”
4323	“Communication time-out error”
4324	“Basic Engine returned error number 0xXX”
3700	“Version: X.Y.Z”
3701	“Parity error from Basic Engine to Serial”
3702	“Unexpected response from Basic Engine”
3703	“Communication time-out error”
3704	“Basic Engine returned error number 0xXX”
5800	Test successful

Error code	Error text
5820	Test successful
5840	Test successful
5860	Test successful
5801	"Unexpected response from Basic Engine"
7000	"Manuf. ID: <XX>" "Device ID: <YY>"
7001	"Comm Test Failed"
7002	"Load Cmd Failed"
7003	"Load Dat Failed"
7004	"Run Cmd Failed"
7100	"ROM Checksum: XXXX"
7101	"Comm Test Failed"
7102	"Load Cmd Failed"
7103	"Load Dat Failed"
7104	"Run Cmd Failed"
7201	"Comm Test Failed"
7200	"Test successful"
7202	"Load Cmd Failed"
7203	"Load Dat Failed"
7204	"Run Cmd Failed"
7205	"Scratch circuit not OK"

5.12.3 Display PWB Nuclei

Error code	Error text
3000	“Test successful”
3001	“Disp not responding”
3002	“Disp key no response”
3003	“One or more patterns not correct”
3004	“Disp type invalid”
3020	“Test successful”
3021	“Disp not responding”
3022	“Disp key no response”
3023	“One or more patterns not correct”
3040	“Test successful”
3041	“Disp not responding”
3042	“Disp key no response”
3043	“One or more patterns not correct”
2700	“Model name in wich the test is running”
2701	“Disp key no response”
2702	“Disp not responding”
2707	“Stop key not pressed”
2708	“Pause key not pressed”
2709	“Play key not pressed”
2710	“Open/close key not pressed”
2713	“Previous key not pressed”
2714	“Next key not pressed”
2715	“More than one key not pressed”
2716	" Audio key not pressed"
2900	“Test successful”
2901	“Slave not responding”
2902	“Slave keyboard not responding”
2903	“Standby led not working”
2800	“Test successful”
2801	“Slave display controller not responding”
2802	“Slave keyboard not responding”
2803	“No key press received from remote control”

Error code	Error text
2600	“The ROM version of the slave processor = 0xXX, and the internal ID = 0xYY”
2601	“I2c bus busy”
2602	“I2c bus not working“
6000	P50 test
6001	“No readback on P50”
6002	“Disp not responding “
6003	“P50 readback error”

5.12.4 Processor & Peripherals Nuclei

Error code	Error text
700	Test successful
720	Test successful
740	Test successful
600	"All checksums are correct"
601	“Following checksum is faulty: BootCode1 Checksum is 0xY2 and is not correct (must be 0xZ2)”
601	“This test is not available when stand-alone compiled”
6200	"Checksums = 0xA1, 0xB1, 0xC1, 0xD1"
6201	“This test is not available when stand-alone compiled”
1000	Test successful
1001	Test successful
1020	Test successful
1021	Test successful
1100	Test successful
1104	“NVRAM reply time-out”
1200	Test successful
1202	“Slave bus not working”
1203	“Slave controller not responding”
1204	“Slave response is not correct”
5900	Test successful
5901	“I2c bus busy”
5902	“I2c bus not working“
5904	“DTS chip response not correct”
1300	Test successful
1301	“Parity error from basic engine to serial”
1302	“Parity error from serial to basic engine”
1303	“No communication between serial and basic engine”
1304	“Communication time-out error”
1600	Test successful
1601	“The DVD SDRAM is faulty”

5.12.5 Log Nuclei

Error code	Error text
3100	"Show error log"
3101	"Error log is invalid"
3102	"Error log could not be read from NVRAM"
3103	"I2C bus busy before start"
3200	"Show error bit"
3201	"Error log is invalid"
3202	"I2C bus busy before start"
3203	"Error log could not be read from NVRAM"
3300	"Error log is cleared"
3301	"Error log could not be cleared"
3302	"I2C bus busy before start"

5.12.6 Miscellaneous Nuclei

Error code	Error text
3400	Test successful
3401	"The configuration data could not be read from NVRAM"
3402	"I2C bus busy before start"
3500	"NVRAM is cleared"
3501	"The NVRAM could not be reset."
3502	"I2C bus busy before start"
3600	"NVRAM contents updated."
	"NVRAM contents and configuration checksum updated."
3601	"NVRAM contents could not be updated."
3602	"I2C bus busy before start"
3603	"NVRAM contents could not be read"
3604	"NVRAM not accessible."
3605	"NVRAM checksum could not be updated."
1500	Test successful
1502	"NVRAM access time-out"
1504	"NVRAM fails"
5400	Test successful
5401	"I2c bus busy"
5402	"I2c bus not working"
5403	"Scart switch controller not responding"
5404	"Scart switch controller response not correct"
5500	Test successful
5501	"I2c bus busy"
5502	"I2c bus not working"
5520	Test successful
5521	"I2c bus busy"
5522	"I2c bus not working"
5523	"Scart switch controller not responding"
5200	Test successful
5201	"I2c bus busy"
5202	"I2c bus not working"
5300	Test successful
5301	"I2c bus busy"
5302	"I2c bus not working"
5320	Test successful
5321	"I2c bus busy"
5322	"I2c bus not working"
4700	"Number of times Tray went Open : XX"
4701	The total number of times tray went open could not be read from NVRAM.
4702	I2C bus busy before start
4720	"Total Power On time (minutes) : XX"
4721	The total power-on time could not be read from NVRAM.
4722	I2C bus busy before start
4740	"Total CDDA & VCD disks Play-time (minutes) : XX"
4741	The playtime of CDDA & VCD disks could not be read from NVRAM.
4742	I2C bus busy before start
4760	"Total DVD disks Play-time (minutes) : XX"
4761	The playtime of DVD disks could not be read from NVRAM.
4762	I2C bus busy before start
4600	"Version of Application Software : XX"
4601	"The application version could not be read from NVRAM."
4602	"I2C bus busy before start"

5.12.7 Video Nuclei

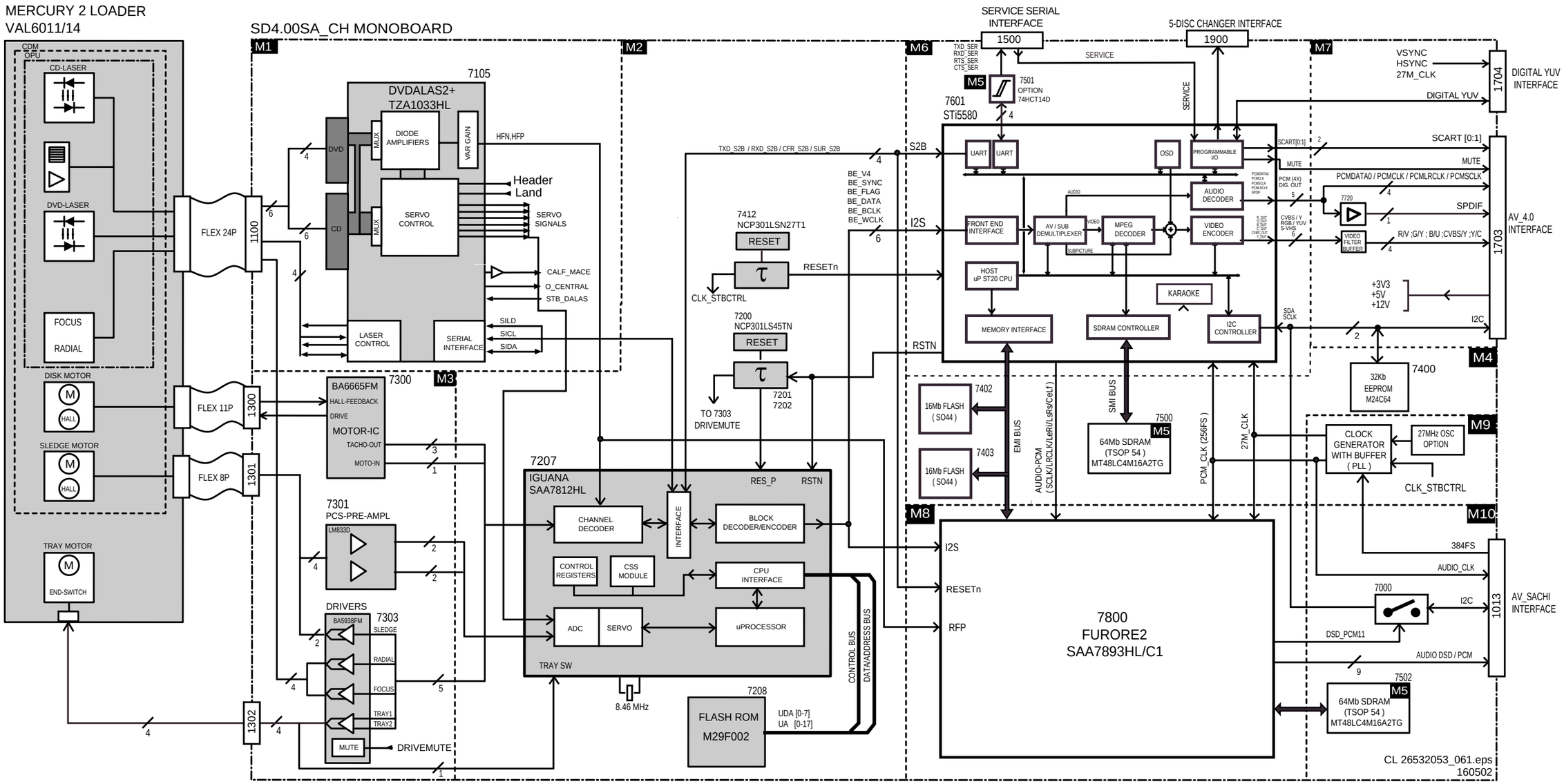
Error code	Error text
2300	Test successful
2320	Test successful
2340	Test successful
2400	Test successful
2401	"I2c bus busy"
2421	"I2c bus busy"
2441	"I2c bus busy"
2500	Test successful
2501	"I2c bus busy"
2502	"I2c bus not working"
2520	Test successful
2521	"I2c bus busy"
2522	"I2c bus not working"
2540	Test successful
2541	"I2c bus busy"
2542	"I2c bus not working"
6100	Test successful
6100	Test successful

5.12.8 Furore Nuclei

Error code	Error text
8300	"Test successful"
8301	"Invalid Version ID read. "
8400	"Test successful"
8420	"Test successful"

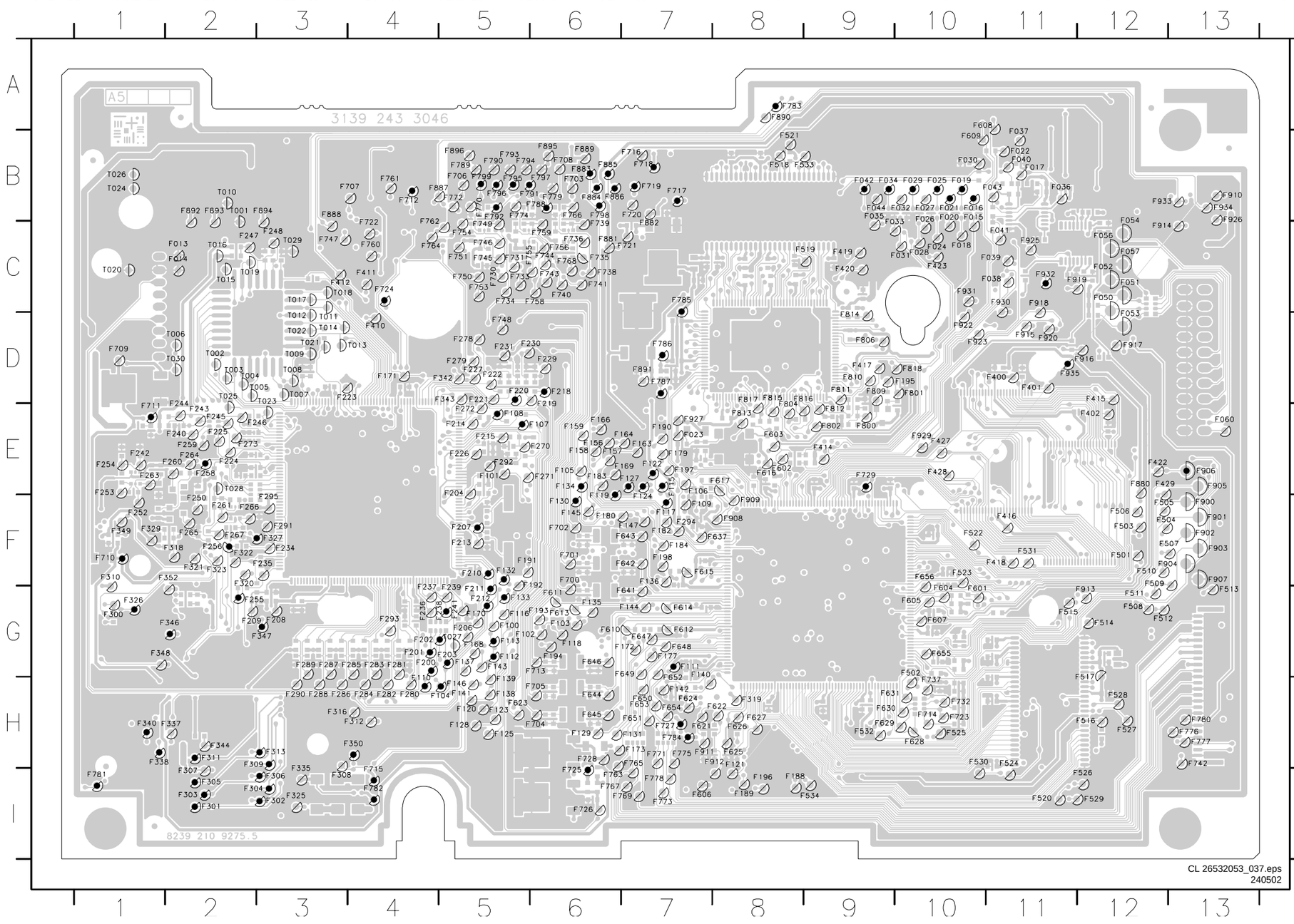
6. Block Diagram

Block Diagram



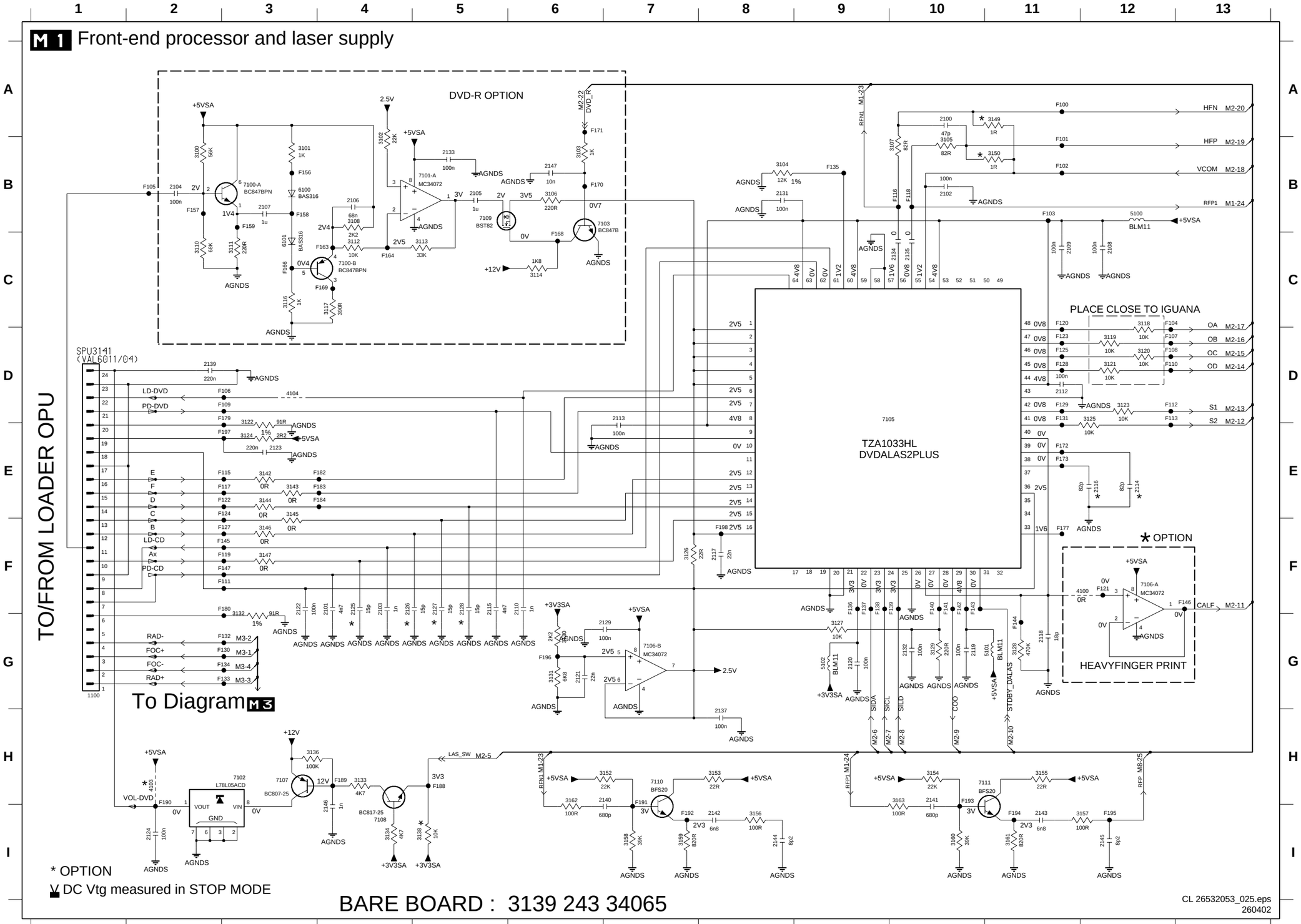
Testpoint Overview

F013 C2	F028 C10	F043 B11	F105 E6	F121 I8	F137 G5	F163 E7	F188 I8	F204 E5	F222 D5	F240 E2	F258 E2	F280 H4	F295 F3	F316 H4	F342 D5	F414 E9	F650 H7	F779 B6	F934 B13
F014 C2	F029 B10	F044 B9	F106 E7	F122 E7	F138 H5	F164 E7	F189 I8	F206 G5	F223 D3	F241 G5	F259 E2	F281 G4	F300 G1	F318 F2	F343 D5	F415 D12	F651 H7	F780 H13	F935 D11
F015 C10	F030 B10	F050 C12	F107 E5	F123 H5	F139 H5	F166 E6	F190 E7	F207 F5	F224 E2	F242 E1	F260 E2	F282 H4	F301 I2	F319 H8	F344 H2	F416 F11	F652 G7	F781 I1	T001 C2
F016 B10	F031 C10	F051 C12	F108 E5	F124 E7	F140 H7	F168 G5	F191 F5	F208 G3	F225 E2	F243 E2	F261 F2	F283 G4	F302 I3	F320 F2	F346 G2	F417 D9	F653 H7	F782 I4	T002 D2
F017 B11	F032 B10	F052 C12	F109 F7	F125 H5	F141 H5	F169 E6	F192 F5	F209 G2	F226 E5	F244 E2	F263 E1	F284 H4	F303 I2	F321 F2	F347 G3	F418 F11	F654 H7	F783 A8	T003 D2
F018 C10	F033 C9	F053 D12	F110 H4	F127 E7	F142 H7	F170 G5	F193 G6	F210 F5	F227 D5	F245 E2	F264 E2	F285 G4	F304 I3	F322 F2	F348 G1	F419 C9	F655 G10	F784 H7	T004 D2
F019 B10	F034 B9	F054 C12	F111 G7	F128 H5	F143 G5	F171 D4	F194 G6	F211 G5	F229 D6	F246 E2	F265 F2	F286 H3	F305 I2	F323 F2	F349 F1	F420 C9	F656 G10	F785 C7	T005 D2
F020 C10	F035 C9	F056 C12	F112 G5	F129 H6	F144 G7	F172 G7	F195 D9	F212 G5	F230 D5	F247 C2	F266 F2	F287 G3	F306 I3	F325 I3	F350 H4	F422 E12	F700 G6	F786 D7	T006 D2
F021 B10	F036 B11	F057 C12	F113 G5	F130 F6	F145 F6	F173 H6	F196 I8	F213 F5	F231 D5	F248 C3	F267 F2	F288 H3	F307 I2	F326 G1	F352 G2	F423 C10	F701 F6	F787 D7	T007 D3
F022 B11	F037 B11	F060 E13	F115 E7	F131 H6	F146 H5	F177 G7	F197 E7	F214 E5	F234 F3	F250 F2	F270 E5	F289 G3	F308 H3	F327 F3	F400 D11	F427 E10	F702 F6	F788 B6	T008 D3
F023 E7	F038 C11	F100 G5	F116 G5	F132 F5	F147 F7	F179 E7	F198 F7	F215 E5	F235 F3	F252 F1	F271 E5	F290 H3	F309 H3	F329 F1	F401 D11	F428 E10	F703 B6	F789 B5	T009 D3
F024 C10	F039 C11	F101 E5	F117 F7	F133 G5	F156 E6	F180 F7	F200 G4	F218 D6	F236 G4	F253 E1	F272 E5	F291 F3	F310 G1	F335 I3	F402 E12	F429 E12	F704 H6	F790 B5	T010 B2
F025 B10	F040 B11	F102 G6	F118 G6	F134 E6	F157 E6	F182 F7	F201 G4	F219 D6	F237 G4	F254 E1	F273 E2	F292 E5	F311 H2	F337 H2	F410 D4	F501 F12	F705 H6	F791 B5	T011 C3
F026 C10	F041 C11	F103 G6	F119 F6	F135 G6	F158 E6	F183 E6	F202 G5	F220 D5	F238 G5	F255 G2	F278 D5	F293 G4	F312 H4	F338 H1	F411 C4	F502 H10	F706 B5	F792 B5	T012 D3
F027 B10	F042 B9	F104 H5	F120 H5	F136 F7	F159 E6	F184 F7	F203 G5	F221 D5	F239 G5	F256 F2	F279 D5	F294 F7	F313 H3	F340 H1	F412 C3	F503 F12	F707 B4	F793 B5	T013 D3
																F504 F12	F708 B6	F794 B5	T014 D3
																F505 F12	F709 D1	F795 B5	T015 C2
																F506 F12	F710 F1	F796 B5	T016 C2
																F507 F13	F711 E1	F797 B6	T017 C3
																F508 G12	F712 B4	F798 B6	T018 C3
																F509 F13	F713 G6	F799 B5	T019 C2
																F510 F12	F714 H10	F800 E9	T020 C1
																F511 G12	F715 I4	F801 D10	T021 D3
																F512 G12	F716 B7	F802 E9	T022 D3
																F513 G13	F717 B7	F804 E8	T023 E3
																F514 G12	F718 B7	F806 D9	T024 B1
																F515 G11	F719 B7	F809 D9	T025 E2
																F516 H12	F720 B7	F810 D9	T026 B1
																F517 G12	F721 C7	F811 D9	T027 G5
																F518 B8	F722 C4	F812 E9	T028 E2
																F519 C9	F723 H10	F813 E8	T029 C3
																F520 I11	F724 C4	F814 D9	T030 D2
																F521 B8	F725 I6	F815 E8	
																F522 F10	F726 I6	F816 E8	
																F523 F10	F727 H7	F817 E8	
																F524 I11	F728 H6	F818 D10	
																F525 H10	F729 E9	F880 E12	
																F526 I12	F730 C5	F881 C6	
																F527 H12	F731 C5	F882 B7	
																F528 H12	F732 H10	F883 B6	
																F529 I11	F733 C5	F884 B6	
																F530 I10	F734 C5	F885 B6	
																F531 F11	F735 C6	F886 B6	
																F532 H9	F736 C6	F887 B4	
																F533 B9	F737 H10	F888 C3	
																F534 I9	F738 C6	F889 B6	
																F601 G10	F739 C6	F890 A8	
																F602 E8	F740 C6	F891 D7	
																F603 E8	F741 C6	F892 C2	
																F604 G10	F742 H13	F893 C2	
																F605 G10	F743 C6	F894 C3	
																F606 I7	F744 C6	F895 B6	
																F607 G10	F745 C5	F896 B5	
																F608 A11	F746 C5	F900 F13	
																F609 B10	F747 C3	F901 F13	
																F610 G7	F748 D5	F902 F13	
																F611 G6	F749 C5	F903 F13	
																F612 G7	F750 C5	F904 F13	
																F613 G6	F751 C5	F905 E13	
																F614 G7	F753 C5	F906 E13	
																F615 F7	F754 C5	F907 F13	
																F616 E8	F755 C6	F908 F8	
																F617 E8	F756 C6	F909 F8	
																F621 H7	F758 C6	F910 B13	
																F622 H8	F759 C6	F911 H7	
																F623 H5	F760 C4	F912 I8	
																F624 H7	F761 B4	F913 G12	
																F625 H8	F762 C5	F914 C13	
																F626 H8	F763 H6	F915 D11	
																F627 H8	F764 C4	F916 D12	
																F628 H10	F765 I7	F917 D12	
																F629 H10	F766 B6	F918 C11	
																F630 H10	F767 I7	F919 C11	
																F631 H10	F768 C6	F920 D11	
																F637 F7	F769 I7	F922 D10	
																F641 G7	F770 B5	F923 D10	
																F642 F7	F771 H7	F925 C11	
																F643 F7	F772 B5	F926 B13	
																F644 H6	F773 I7	F927 E7	
																F645 H6	F774 B5	F929 E10	
																F646 G6	F775 H7	F930 C11	
																F647 G7	F776 H13	F931 C10	
																F648 G7	F777 H13	F932 C11	
																F649 G7	F778 I7	F933 B13	



7. Electrical Diagrams and PWB's

Front-End Processor and Laser Supply



1100 G1	7103 B6
2100 A10	7105 D9
2101 F4	7106-A F12
2102 B10	7106-B G7
2103 F4	7107 H3
2104 B2	7108 I4
2105 B5	7109 B5
2106 B4	7110 H7
2107 B3	7111 H10
2108 C12	F100 A11
2109 C11	F101 B11
2110 F6	F102 B11
2112 D11	F103 B11
2113 D7	F104 C12
2114 E12	F105 B2
2115 F5	F106 D3
2116 E12	F107 D12
2117 F8	F108 D12
2118 G11	F109 D3
2119 G10	F110 D12
2120 G9	F111 F3
2121 G6	F112 D12
2122 F3	F113 D12
2123 E3	F115 E3
2124 I2	F116 B10
2125 F4	F117 E3
2126 F4	F118 B10
2127 F5	F119 F3
2128 F5	F120 C11
2129 G7	F121 F12
2131 B8	F122 E3
2132 G10	F123 D11
2133 B5	F124 E3
2134 C10	F125 D11
2135 C10	F127 F3
2137 H8	F128 D11
2139 D2	F129 D11
2140 H7	F130 G3
2141 H10	F131 D11
2142 I8	F132 G3
2143 I11	F133 G3
2144 I8	F134 G3
2145 I12	F135 B9
2146 I4	F136 F9
2147 B6	F137 F9
3100 B2	F138 F9
3101 B3	F139 F10
3102 B4	F140 F10
3103 B6	F141 F10
3104 B8	F142 F10
3105 B10	F143 F10
3106 B6	F144 G11
3107 B10	F145 F3
3108 B4	F146 F13
3110 C2	F147 F3
3111 C3	F156 B3
3112 C4	F157 B2
3113 C5	F158 B3
3114 C6	F159 B3
3116 C3	F163 C4
3117 C4	F164 C4
3118 C12	F166 C3
3119 D12	F168 B6
3120 D12	F169 C4
3121 D12	F170 B6
3122 E3	F171 A6
3123 D12	F172 E11
3124 E3	F173 E11
3125 D12	F177 F11
3126 F7	F179 D3
3127 G9	F180 E3
3128 G11	F182 E4
3129 G10	F183 E4
3130 G6	F184 E4
3131 G6	F188 H5
3132 G3	F189 H4
3133 H4	F190 H2
3134 I4	F191 H7
3136 H3	F192 I7
3138 I5	F193 H10
3142 E3	F194 I11
3143 E3	F195 I12
3144 E3	F196 G6
3145 E3	F197 E3
3146 F3	F198 F8
3147 F3	
3149 A11	
3150 B11	
3152 H7	
3153 H8	
3154 H10	
3155 H11	
3156 I8	
3157 I12	
3158 I7	
3159 I7	
3160 I10	
3161 I11	
3162 H6	
3163 H10	
4100 F12	
4103 H2	
4104 D3	
5100 B12	
5101 G11	
5102 G9	
6100 B3	
6101 C3	
7100-A B3	
7100-B C4	
7101-A B5	
7102 H3	

Front-End Processor Iguana

M2

Front-end Processor IGUANA

FOR DEBUGGING

7207
SAA7812HL
IGUANA

Decoupling Cap For 7200 (SAA7812HL IGUANA)

NCP301LSN45T

SCRATCH DETECTOR OPTION

ICE Interface

AFTER PROTOTYPE CHECK S'WARE

BARE BOARD : 3139 243 34065

CL 26532053_026.eps
260402

* OPTION

\# Connection to ICE Interface

V DC vtg measured in Stop-Mode

1200	A3	3289	M15
1201	G3	3290	M15
2200	B12	3291	M15
2201	B12	3293	N24
2202	B13	3294	P9
2203	B13	4200	N9
2204	C12	4201	P11
2205	C12	4203	C23
2206	F14	4204	D14
2207	C13	4205	D13
2208	C13	5200	D5
2209	C14	5201	D5
2210	E14	5202	H2
2211	E14	5203	I19
2212	C15	5204	I20
2213	C15	7101-B	M23
2214	C16	7200	B19
2215	D3	7201	C21
2216	E23	7202-A	E22
2217	E3	7202-B	D24
2218	F23	7203-A	D18
2219	G3	7203-B	E20
2220	G3	7204	D20
2221	I20	7207	I10
2222	J15	7208	I19
2223	M14	7209	N22
2224	M14	F200	C6
2225	M16	F201	C6
2226	M16	F202	C6
2227	N2	F203	C6
2228	N2	F204	I5
2229	N3	F206	E4
2230	N4	F207	G5
2231	N4	F208	E5
2232	N4	F209	E5
2233	N22	F210	F5
2234	P3	F211	F5
2235	P3	F212	G5
2236	P3	F213	G5
2237	P4	F214	L5
2238	P4	F215	K5
2239	I3	F218	O6
2240	M24	F219	O6
2241	N24	F220	O6
3200	A7	F221	O6
3201	A10	F222	P6
3202	B20	F223	O10
3203	A8	F224	K14
3204	A10	F225	K14
3205	B7	F226	K5
3206	B10	F227	K5
3207	B20	F229	O3
3208	B8	F230	O3
3209	B10	F231	O3
3210	B7	F234	G15
3211	B10	F235	F15
3212	B8	F236	E7
3213	B10	F237	E7
3214	B21	F238	E7
3215	C7	F239	E6
3216	C10	F240	K15
3217	C8	F241	E5
3218	C10	F242	F20
3219	C23	F243	K15
3221	C7	F244	L15
3222	C10	F245	K14
3223	C8	F246	L14
3224	C10	F247	I18
3225	D20	F248	P18
3226	D22	F250	B19
3227	D7	F252	D18
3228	D10	F253	E18
3229-A	D6	F254	E19
3233	D18	F255	F16
3234	D20	F256	G16
3235	D7	F258	K15
3236	D21	F259	K15
3237	D23	F260	D21
3238	E18	F261	D23
3239	E23	F263	D20
3240	E19	F264	C20
3241	E24	F265	D21
3242	F4	F266	E24
3243	F19	F267	D22
3244	F20	F270	K4
3245	F15	F271	M22
3246	G15	F272	M21
3247	G4	F273	M24
3250	I4	F278	N6
3251	J18	F279	N6
3252-B	I15	F280	D8
3255	J2	F281	D8
3256	J14	F282	D8
3257-D	K15	F283	D8
3261	L23	F284	D9
3262	L22	F285	D9
3263	N5	F286	D9
3265	N22	F287	D9
3266	N20	F288	D9
3267	O5	F289	D9
3268	O5	F290	D9
3270	O5	F291	G15
3271	O5	F292	N22
3272	N5	F293	D23
3273	P5	F294	P10
3274	O11	F295	D14
3275	P7		
3277	P10		
3278	P10		
3279	P11		
3280	P7		
3282	Q7		
3283	N11		
3284	I4		
3287	L5		
3288	M15		

Front-End Loader Interface

M3 Front-end Loader Interface

DISC MOTOR CONTROL
TO / /FROM LOADER

SLEDGE MOTOR CTRL
TO / /FROM LOADER

TRAY MOTOR
TO / /FROM LOADER

DISC TYPE	3345	3323
SINGLE DISC	X	✓
5-DISC CHANGER	✓	X

* OPTION

V DC Vtg measured in STOP MODE

BARE BOARD : 3139 243 34065

CL 26532053_027.eps
260402

1300 A2	F322 G2
1301 F2	F323 G2
1302 I2	F325 A14
2300 A11	F326 F2
2301 B14	F327 F2
2302 D14	F329 F13
2303 D13	F335 B14
2304 D5	F337 J2
2305 E9	F338 J2
2306 F9	F340 J2
2307 K12	F342 K10
2308 K3	F343 K10
2309 K4	F344 D2
2310 K4	F346 E5
2311 K14	F347 H5
2312 F5	F348 D5
2313 H2	F349 G4
2314 I5	F350 C13
2315 F14	F352 H13
2316 F15	
2317 A6	
2318 A7	
2319 A8	
2320 F13	
2321 D5	
2322 G8	
2323 H8	
3300 A13	
3301 A13	
3302 A14	
3304 C3	
3305 C16	
3306 D13	
3307 D14	
3308 D3	
3309 D16	
3310 D4	
3312 F4	
3313 G4	
3315 G13	
3316 G13	
3317 H13	
3319 I4	
3321 K13	
3322 I16	
3323 I4	
3324 I14	
3325 J16	
3326 J14	
3327 J14	
3328 K15	
3332 D6	
3333 D7	
3334 D7	
3336 J15	
3337 J15	
3338 A15	
3339 E14	
3340 H13	
3341 H8	
3342 F11	
3343 H14	
3344 H16	
3345 K5	
3346 A14	
4301 C13	
4303 G16	
4304 G16	
5300 J3	
5301 J3	
5302 J3	
6300 B15	
6301 B16	
6302 A16	
7300 A9	
7301-A G5	
7301-B E4	
7303 F9	
7305 F14	
F300 H9	
F301 A2	
F302 A2	
F303 B2	
F304 B2	
F305 B2	
F306 B2	
F307 C2	
F308 C13	
F309 C2	
F310 I8	
F311 C2	
F312 C13	
F313 C2	
F316 C13	
F318 J14	
F319 H2	
F320 H2	

Memory

M4 MEMORY

TO M6

+3V3M1
F400
2405 100n
7402 Am29LV160B 37 VCC
A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15|A-1
RY|BY_ F428
NC2 NC3 NC4
M4-146 CE_ROM1N F401 3V
M6-79 FLASH_OEN F402 0V
3401 10K
RWN
CE_ OE_ WE_ RESET_ BYTE_
VSS1 VSS2
+3V3M1

+3V3M1
2402 100n
7403 Am29LV160B 37 VCC
A21
M4-147 CE_ROM2N F415 3V
M6-79 FLASH_OEN 0V
3403 10K
+3V3M1

VCC_DRAM
100n 2400
100n 2403
100n 2401
7401 GM71V18163CJ
1M X 16
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
RAS0ND CAS0ND CAS1ND RWN OEND RAS1ND F413
RAS_ LCAS_ UCAS_ WE_ OE_
NC3
SDM OPTION

+5V +3V3D
4400 0R
4401 * 0R
F410
2408 100n
7400 M24C64 8 VCC
E0 E1 E2 SCL WC_ VSS
M6-86 SDA F411 5 4V
M6-87 SCL F412
4V

+3V3
5401 F416 100MHZ BLM311 +3V3M1
2410 100u
+3V3 5403 F418 100MHZ BLM311 VCC_DRAM
2412 100u
5402 F417 100MHZ BLM311 VCC_LVC00
2411 100u

+3V3ST
3405 2K2
3404 22K 0V
7404 BC847B
3402 100K
3V F422 RESETn M6-78, M8-78
2413 * 100n
2414 100n

+3V3ST
2415 F419 1u
3412 4K7
0V 7409 BC847B
3406 22K
6400 BAS316
F420 3407 10K
1V4
2417 10u
3411 22K
7405 BC847B 0V 0V6
3413 22K
7413 BC857B 2V4
+3V3ST
3V F423 CLK_STBCTRL M9-148
3414 22K
2418 470n
RESET_ IN GND NC
+3V3ST
7412 NCP301LSN27T1

VCC_LVC00
3409 10K *
A21 F427 0V
7406-A 74LVC00APW
7406-C 74LVC00APW
7406-D 74LVC00APW
7406-B 74LVC00APW
3V CE_ROM2N M4-147
M6-131 CE_ROMN * 4405 F414 CE_ROM1N M4-146

* OPTION
V DC Vtg measured in STOP MODE

BARE BOARD : 3139 243 34065

CL 26532053_028.eps
260402

2400 B11
2401 B13
2402 B9
2403 B11
2405 B4
2408 B16
2410 E17
2411 G17
2412 F15
2413 I16
2414 I17
2415 I11
2417 J13
2418 K16
3401 H1
3402 H16
3403 H6
3404 H16
3405 H15
3406 J12
3407 I14
3409 J2
3411 J14
3412 J11
3413 I16
3414 K16
4400 A16
4401 A16
4405 K4
5401 E17
5402 F17
5403 E14
6400 I13
7400 B15
7401 B11
7402 B3
7403 B7
7404 I16
7405 I14
7406-A J3
7406-B J8
7406-C J5
7406-D J6
7409 J12
7412 K14
7413 J16
F400 B4
F401 H2
F402 H2
F410 B16
F411 C15
F412 D17
F413 H11
F414 K6
F415 H7
F416 E17
F417 F17
F418 E15
F419 J11
F420 I13
F422 H17
F423 J16
F427 K2
F428 G5
F429 G9

Memory and Service Interface

M5 MEMORY & SERVICE INTERFACE

FURORE SDRAM

TO M8 SACD DECODER

FUR_3V3

5502 0R0 BLM31HB

F533 3507 10K F521 2500 47u

2501 100n, 2504 100n, 2507 100n, 2510 100n, 2513 100n, 2516 100n, 2517 100n

7502 MT48LC4M16A2TG

1 14 27 3 9 43 49

VDD VDDQ

CTRL LOGIC, COMMAND DECODE, MODE REG, REFRESH COUNTER, ROW ADDR MUX, BANK CTRL LOGIC, COLUMN ADDR COUNTER/ LATCH, COLUMN DEDCODER, ADDRESS REGISTER

BANK0 ROW-ADDR LATCH & DECODER

BANK0 MEMORY ARRAY (4,096x256x16)

SENSE AMPLIFIERS, I/O GATING DQM DATA LOGIC READ DATA LATCH WRITE DRIVERS, DQML DQMH

DATA OUTPUT REGISTER, DATA INPUT REGISTER

F518	CLK	38			
F519	CS	19			
	CKE	37			
FUR_WEn	WE	16	DQML	15	FUR_DQML
FUR_CASn	CAS	17	DQMH	39	FUR_DQMH
FUR_RASn	RAS	18	DQ0	2	FUR_DQ0
FUR_AD12	BA0	20	DQ1	4	FUR_DQ1
FUR_AD13	BA1	21	DQ2	5	FUR_DQ2
FUR_AD0	A0	23	DQ3	7	FUR_DQ3
FUR_AD1	A1	24	DQ4	8	FUR_DQ4
FUR_AD2	A2	25	DQ5	10	FUR_DQ5
FUR_AD3	A3	26	DQ6	11	FUR_DQ6
FUR_AD4	A4	29	DQ7	13	FUR_DQ7
FUR_AD5	A5	30	DQ8	42	FUR_DQ8
FUR_AD6	A6	31	DQ9	44	FUR_DQ9
FUR_AD7	A7	32	DQ10	45	FUR_DQ10
FUR_AD8	A8	33	DQ11	47	FUR_DQ11
FUR_AD9	A9	34	DQ12	48	FUR_DQ12
FUR_AD10	A10	22	DQ13	50	FUR_DQ13
FUR_AD11	A11	35	DQ14	51	FUR_DQ14
			DQ15	53	FUR_DQ15

3508 1K

VSSQ 6 12 46 52, VSS 28 41 54, NC 36 40

ST SDRAM

+3V3_ST_MEM

F516 3502 10K

2505 100n, 2506 100n, 2511 100n, 2512 100n, 2518 100n, 2519 100n, 2520 100n

7500 MT48LC4M16A2TG

1 14 27 3 9 43 49

VDD VDDQ

CTRL LOGIC, COMMAND DECODE, MODE REG, REFRESH COUNTER, ROW ADDR MUX, BANK CTRL LOGIC, COLUMN ADDR COUNTER/ LATCH, COLUMN DEDCODER, ADDRESS REGISTER

BANK0 ROW-ADDR LATCH & DECODER

BANK0 MEMORY ARRAY (4,096x256x16)

SENSE AMPLIFIERS, I/O GATING DQM DATA LOGIC READ DATA LATCH WRITE DRIVERS, DQML DQMH

DATA OUTPUT REGISTER, DATA INPUT REGISTER

	CKE	37			
CLK	CLK	38			
CSN1	CS	19			
WEN	WE	16			
CASN	CAS	17			
RASN	RAS	18			
			DQML	15	DQML
			DQMH	39	DQMU
AD13	BA0	20	DQ0	2	DQ7
AD12	BA1	21	DQ1	4	DQ6
AD0	A0	23	DQ2	5	DQ5
AD1	A1	24	DQ3	7	DQ4
AD2	A2	25	DQ4	8	DQ3
AD3	A3	26	DQ5	10	DQ2
AD4	A4	29	DQ6	11	DQ1
AD5	A5	30	DQ7	13	DQ0
AD6	A6	31	DQ8	42	DQ15
AD7	A7	32	DQ9	44	DQ10
AD8	A8	33	DQ10	45	DQ11
AD9	A9	34	DQ11	47	DQ12
AD10	A10	22	DQ12	48	DQ13
AD11	A11	35	DQ13	50	DQ14
			DQ14	51	DQ9
			DQ15	53	DQ8

VSSQ 6 12 46, VSS 28 41 54, NC 36 40

+3V3 5505 0805 BLM31HB F517 +3V3_ST_MEM

2524 100n, 2525 47u

TO M6 Back-end Host Processor Share Memory Interface (SMI) Bus

To / From PC Interface

SERVICE 1500

F512 550A 100MHZ BLM11HB +5VD

+5VD 3501 1K

0V 7508-B BC847BS 3503 4K7 F501 TXD_SER M6-89

3504 4K7 F503 +3V3D 3505 10K

F502 3V RXD_SER M6-90

0V 7508-A BC847BS 3506 10K

F504 SERVICE M6-88

F505 3509 100R F506 TXD_SER M6-89

F507 3510 10K F508 3511 330R RXD_SER M6-90

F510 3514 100R F511 RTS_SER M6-98

F513 3516 10K F514 F515 3517 330R F531 CTS_SER M6-127

3512 6K8, 3513 680R, 3515 10K, 3518 6K8, 3519 68R

2521 100n, 2522 1n5, 2523 1n5

7501-A 74HCT14PW, 7501-B 74HCT14PW, 7501-C 74HCT14PW, 7501-D 74HCT14PW, 7501-E 74HCT14PW, 7501-F 74HCT14PW

* OPTION

I2C SLAVE OPTION

RWN, A1

+5VI2C: 2528 100n, 3520 10K, 3521 10K, 3524 10K

+5VD: 5501 100MHZ BLM11, F532 +5VI2C, 2526 100n

7504 PCF8584T

M6-132	RESET_I2C	F523	RESET_|STROBE_	19	
M6-130	CE1	F523	CS_	17	
			A0	6	
			WR_	18	
M5-168	DTACKn	F524	RD_	16	
M6-169	IRQ_I2C	F525	INT_|SCL-OUT	5	
			IACK_|SDA-IN	4	
M5-170	CLK_8MHZ		CLK	1	
M7-141	SDA_EXE		SDA|SDA-OUT	2	
M7-142	SCL_EXE		SCL|SCL-IN	3	

3522 100R, 3523 100R

VDD 20, VSS 10

7505 74LVC245APW

G3 VCC 19 20, 3EN1 GND 1 10, 3EN2 2 18

+3V3D 2527 100n

D7 D6 D5 D4 D3 D2 D1 D0

TO DIAGRAM M6

7506-A 74LVC00APW F527 7506-B 74LVC00APW 3529 10K F528

7506-C 74LVC00APW 7506-D 74LVC00APW 2529 100n

DTACKn, CE1, WAIT_SLAVE_I2C, WAIT_FUR, WAIT_I2C_FUR

7509-3 74LVC02APW, 7509-4 74LVC02APW, 7509-1 74LVC02APW, 7509-2 74LVC02APW

4500, 3531 47K, 3530 10K, CSL_FUR F534

M5-168, M6-130, M6-164, M6-191, M6-171

7507-A 74HCU04PW, 7507-B 74HCU04PW, 7507-C 74HCU04PW, 7507-D 74HCU04PW, 7507-E 74HCU04PW, 7507-F 74HCU04PW

3526 1M, 3527 4R7 +3V3D, 2532 100n, F530, F520, F526, F529

3529 560R, 1501 8M CSTCC, 2530 22p, 2531 22p

CLK_8MHZ M5-170

OPTION

DC Vtg measured in STOP MODE * OPTION

BARE BOARD : 3139 243 34065

CL 26532053_029.eps 260402

1500	G17	F528	N13
1501	P22	F529	P23
2500	C6	F530	O23
2501	C4	F531	J23
2504	C6	F532	M6
2505	C12	F533	C3
2506	C14	F534	P19
2507	D4		
2510	D6		
2511	C12		
2512	C14		
2513	D4		
2516	D6		
2517	D6		
2518	D12		
2519	D14		
2520	D12		
2521	E21		
2522	F18		
2523	I20		
2524	L12		
2525	L13		
2526	N6		
2527	M9		
2528	M2		
2529	O13		
2530	P21		
2531	P23		
2532	O25		
2533	O18		
3501	B20		
3502	B12		
3503	B21		
3504	C21		
3505	C22		
3506	D22		
3507	C4		
3508	K2		
3509	F19		
3510	G19		
3511	G22		
3512	H18		
3513	H23		
3514	H20		
3515	I23		
3516	J20		
3517	J23		
3518	J20		
3519	J23		
3520	N2		
3521	N3		
3522	P4		
3523	P3		
3524	N3		
3526	N22		
3527	N24		
3528	P23		
3529	N14		
3530	P19		
3531	P15		
4500	N17		
5501	M5		
5502	C5		
5504	J17		
5505	K12		
7500	E12		
7501-A	F22		
7501-B	H22		
7501-C	G20		
7501-D	J22		
7501-E	K21		
7501-F	K22		
7502	E3		
7504	N4		
7505	L7		
7506-A	N11		
7506-B	N12		
7506-C	O11		
7506-D	O12		
7507-A	O22		
7507-B	O24		
7507-C	M20		
7507-D	M21		
7507-E	M22		
7507-F	M24		
7508-A	D22		
7508-B	B21		
7509-1	P16		
7509-2	Q18		
7509-3	N16		
7509-4	M18		
F501	B23		
F502	C23		
F503	C21		
F504	E21		
F505	F18		
F506	F19		
F507	G18		
F508	G21		
F509	G19		
F510	H20		
F511	H21		
F512	I18		
F513	J20		
F514	J21		
F515	J22		
F516	B11		
F517	K14		
F518	F3		
F519	F3		
F520	O23		
F521	C4		
F522	N3		
F523	N3		
F524	O3		
F525	O3		
F526	O23		
F527	N12		

Back-End Host Processor

M6 Back-end Host Processor

	VDDSTA	VDDSTC	VDDSTD
STi5580	+2V5	+2V5	+2V5
STi5588	+1V8	+1V8	+3V3
STi5519	+2V5	+2V5	+2V5

To Diagram **M4** **M5** **M8**

EMI Bus

7601 STi5580

MEMORY interface

SYSTEM USE

PORT 0 I/O

PORT 1 I/O

PORT 2 I/O

PORT 3 I/O

PORT 4 I/O

JTAG

IRQ

uP ST20cpu

A/V/Sub demultiplexer

MPEG DECODER

Subpicture decoder

AC3 LPCM MPEG1/2 DTS

AUDIO DECODER

KARAOKE

VIDEO ENCODER

FRONT-END Interface

I^2S

SDRAM CONTROLLER

ADDRESS

DATA

SMI Bus

To **M5** Back-end SDRAM and Service Interface

BARE BOARD : 3139 243 34065

* OPTION

DC Vtg measured in STOP MODE

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Power Supply & A/V Interface

M 7 POWER SUPPLY & A/V INTERFACE

To Display Board

ANALOG VIDEO & I2S AUDIO OUTPUT

To 5 Disc Changer PSU

I2S KARAOKE INPUT

DIGITAL YUV VIDEO OUTPUT

OPTION

* OPTION

V DC Vtg measured in STOP MODE

BARE BOARD : 3139 243 34065

	7704	7707	5707	5725
STI5580	LF25ABDT	LF25ABDT	✓	
STI5588	LF33ABDT	LF18ABDT		✓
STI5519	LF25ABDT	LF25ABDT	✓	

CL 26532053_031.eps
260402

1701 N1
1702 E23
1703 D1
1704 I23
1705 A1
2700 B15
2701 B3
2702 B14
2703 C12
2704 C13
2705 C3
2706 D6
2707 D7
2708 D15
2709 E14
2710 F7
2711 E12
2712 E13
2713 G7
2714 G8
2715 E4
2716 E4
2717 C23
2718 G15
2719 D23
2720 G14
2721 H12
2722 H13
2723 I7
2724 J15
2725 J14
2726 K12
2727 K13
2728 K7
2729 L7
2730 L7
2731 L15
2732 M14
2733 M12
2734 M13
2735 N6
2736 N8
2737 L4
2738 M3
2739 O15
2740 O6
2741 O7
2742 O14
2743 P12
2744 P13
2745 K9
2746 K9
2747 N8
2748 D9
2749 I9
2750 I9
2751 I8
3700 C9
3701 A9
3702 C7
3703 A7
3704 B15
3705 B16
3706 B9
3707 B16
3708 C16
3709 C18
3710 C12
3711 C13
3712 C15
3713 C9
3714 C15
3715 D15
3716 D16
3717 E16
3718 E16
3719 E18
3720 E12
3721 E13
3722 E15
3723 F15
3724 B22
3725 C22
3726 G15
3727 G16
3728 G16
3729 H16
3730 H18
3731 H12
3732 H13
3733 H15
3734 H15
3735 J15
3736 J16
3737 J16
3738 J16
3739 J18
3740 K12
3741 K13
3742 K15
3743 K15
3744 L15
3745 L16
3746 M16
3747 M16
3748 M18
3749 M12
3750 M13
3751 M15
3752 N15
3753 L3
3754 O15
3755 O16
3756 O16
3757 P16
3758 P18
3759 P12
3760 P13
3761 P15
3762 P15
3763-D J4
3764 B7
3765 C7
3766 A8
3767 C8
3768 C21
3769 D21
3770 N3
3771 N3
3772 I3
3773 I3
3774 O3
3775 H3
5700 A4
5701 B13
5702 C4
5703 C9
5704 D9
5705 E8
5706 E13
5707 F8
5708 G8
5709 B23
5710 D23
5712 G13
5713 H8
5714 H8
5715 J13
5716 J8
5717 K8
5718 L8
5719 L8
5720 M8
5721 M8
5722 M13
5723 L4
5724 O13
5725 F8
5726 M21
7700 A7
7701-A B16
7701-B B17
7703 C8
7704 E7
7705-A E16
7705-B E17
7707 F7
7708 B21
7709-A H16
7709-B G17
7710 D22
7713 H7
7714-A J16
7714-B J17
7716 J6
7717-A M16
7717-B L17
7719 M6
7720 M5
7721-A O16
7721-B O17
7700 B13
7701 E13
7702 G13
7703 I3
7704 J13
7705 M13
7706 E3
7707 B2
7708 I3
7709 J8
7710 J9
7711 K9
7712 C4
7713 O13
7714 F22
7715 L9
7716 K2
7717 L9
7718 M9
7719 K2
7720 L4
7721 M9
7722 B22
7723 F22
7724 C9
7725 E9
7726 E8
7727 F9
7728 G8
7729 G9
7730 E16
7731 E17
7732 G22
7733 E14
7734 F16
7735 J16
7736 J17
7737 G22
7738 J14
7739 K16
7740 B16
7741 B17
7742 G22
7743 B14
7744 C16
F745 O16
F746 O17
F747 D22
F748 O14
F749 P16
F750 G16
F751 G17
F753 G14
F754 H16
F755 L16
F756 L17
F758 M14
F759 N16
F760 B8
F761 A4
F762 C8
F763 K21
F764 E17
F765 L21
F766 J17
F767 L21
F768 B17
F769 M21
F770 P17
F771 M21
F772 H17
F773 N21
F774 M17
F775 O21
F776 J21
F777 J21
F778 N21
F779 E3
F780 K21
F781 H4
F782 I4
F783 I4
F784 D9
F785 M8
F786 H9
F787 H9
F788 H3
F789 J3
F790 G3
F791 H3
F792 G3
F793 G3
F794 F3
F795 G3
F796 F3
F797 F3
F798 J3
F799 F3
F880 H4
F881 H5
F882 I4
F883 J3
F884 J3
F885 K3
F886 K3
F887 B23
F888 D23
F889 I4
F890 I5
F891 H7
F892 N3
F893 N3
F894 O3
F895 H3
F896 E3

SACD Decoder

M8 SACD DECODER

To M6 Back-end Host Processor

To M5 Memory & Service Interface (Furore SDRAM)

To M5 Memory & Service Interface (Furore SDRAM)

To M10 DAC Interface and M6 Back-end Host Processor

To M2 Front-end Processor IGUANA

FURORE2

* OPTION

DC Vtg measured in STOP MODE

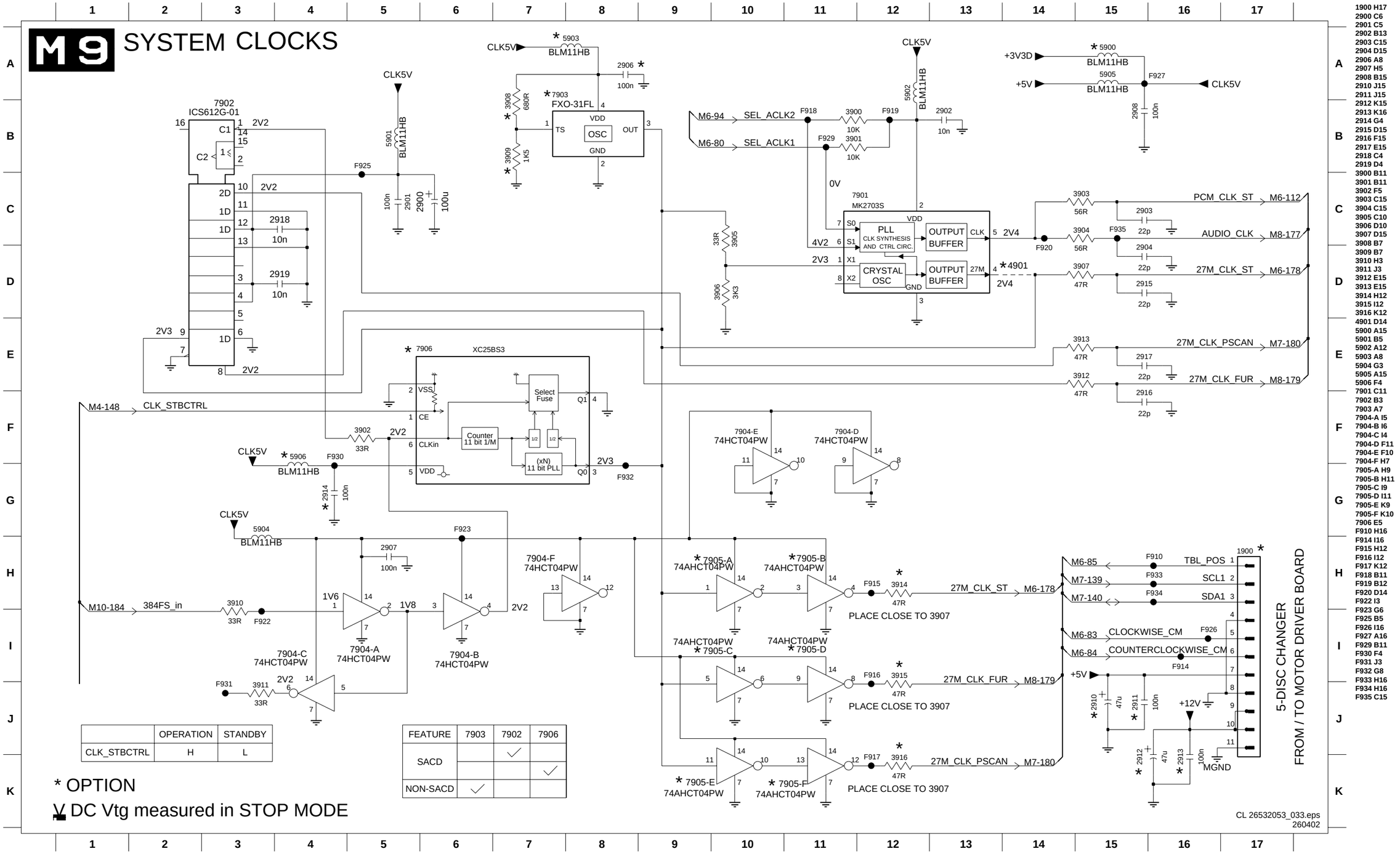
33.8688MHz

BARE BOARD : 3139 243 34065

CL 26532053_032.eps
260402

System Clocks

M9 SYSTEM CLOCKS



	OPERATION	STANDBY
CLK_STBCTRL	H	L

FEATURE	7903	7902	7906
SACD		✓	
NON-SACD	✓		✓

* OPTION

⚓ DC Vtg measured in STOP MODE

Over Sampling	FS	Frequency Audio_CLK	SEL_ACLK2	SEL_ACLK1
256FS	96KHZ	24.576MHZ	1	1
	44.1KHZ	11.2896MHz	1	0
	48KHZ	12.288MHZ	0	0
384FS	44.1KHZ	16.9344MHz		

CLK FACTORY FOR AUDIO_CLK	3914 3915	7901	3900	3901	5902	2902	7905	3903	3904
STi5580 GENERATED	✓		✓				✓	✓	✓
EXTERNAL		✓	✓	✓	✓	✓			

BARE BOARD : 3139 243 34065

DAC Interface

M10 DAC INTERFACE

FUNCTION	3037	3038	4001	4014
DCU		✓		✓
BST	✓		✓	

FOR BScan or DCU

1014 RF

3036 10K FUR_3V3
3010 10K FUR_3V3
3037-A / *3038-D F053 FUR_TMS / ST_TMS
3037-B / *3038-C F050 FUR_TCK / TCK
3008 10K FUR_3V3
3037-C / *3038-B F051 FUR_TDI / ST_TDI
3037-D / *3038-A F052 FUR_TDO / TDO
F056 RESETn
F060 *4001 F054 FUR_TRST
3003 10K
2000 220n *4014 ST_TRST
F057

F017
F022 4005 F023
*7000-A 74HCT4066PW
*7000-C 74HCT4066PW
*2007 100n
SCL 3023 33R 4V 0V *3025 47K CLK5V
FUR_3V3 *3033 10K
M8-163 DSD_PCM11 F036
*7000-B 74HCT4066PW
*7000-D 74HCT4066PW
M6-86 SDA 3029 33R 4V 0V 2V *3031 47K CLK5V
*3032 1K
F041 4006 F043
CLK5V

EMC Holes F013 F014

M6-96 GPIO1 F037
M6-82 GPIO3 F038
M6-81 GPIO2 F039
M8-161 DSD_PCM9 *3034 33R *2015 22p F040
M6-97 P50
M8-160 DSD_PCM8 *3035 33R *2014 22p F030
M6-93 PCMDATA3
STANDBYn
SDA_DAC
SCL_DAC
*1012

M8-167 AUDIO_CLK F015 3019 33R F016 *2004 22p 256Fs
M8-158 DSD_PCM6 F018 3020 33R F019 *2005 22p BIT_CLK/DSD_CLK
M8-159 DSD_PCM7 F020 3021 33R F021 *2006 22p WORD_CLK/SEL_DSD
M8-152 DSD_PCM0 F024 3022 33R F025 *2008 22p DATA_LR/DSD_LEFT
M8-153 DSD_PCM1 F026 3024 33R F027 *2009 22p SEL_PCM/DSD_RIGHT
M6-111 PCM_LsRs_FUR *4007
M8-156 DSD_PCM4 F028 3026 33R F029 *2010 22p DATA_LsRs/DSD_Ls
M8-157 DSD_PCM5 F031 3027 33R F032 *2011 22p SEL_PCM/DSD_Rs
M6-110 PCM_CeLf_FUR *4008
M8-154 DSD_PCM2 F033 3028 33R F034 *2012 22p DATA_CL/DSD_CENTRE
M8-155 DSD_PCM3 F035 3030 33R F044 *2013 22p SEL_PCM/DSD_LFE
384FS_in F042 384Fs
M9-184

1013

TO/FROM DAC BOARD

* OPTION

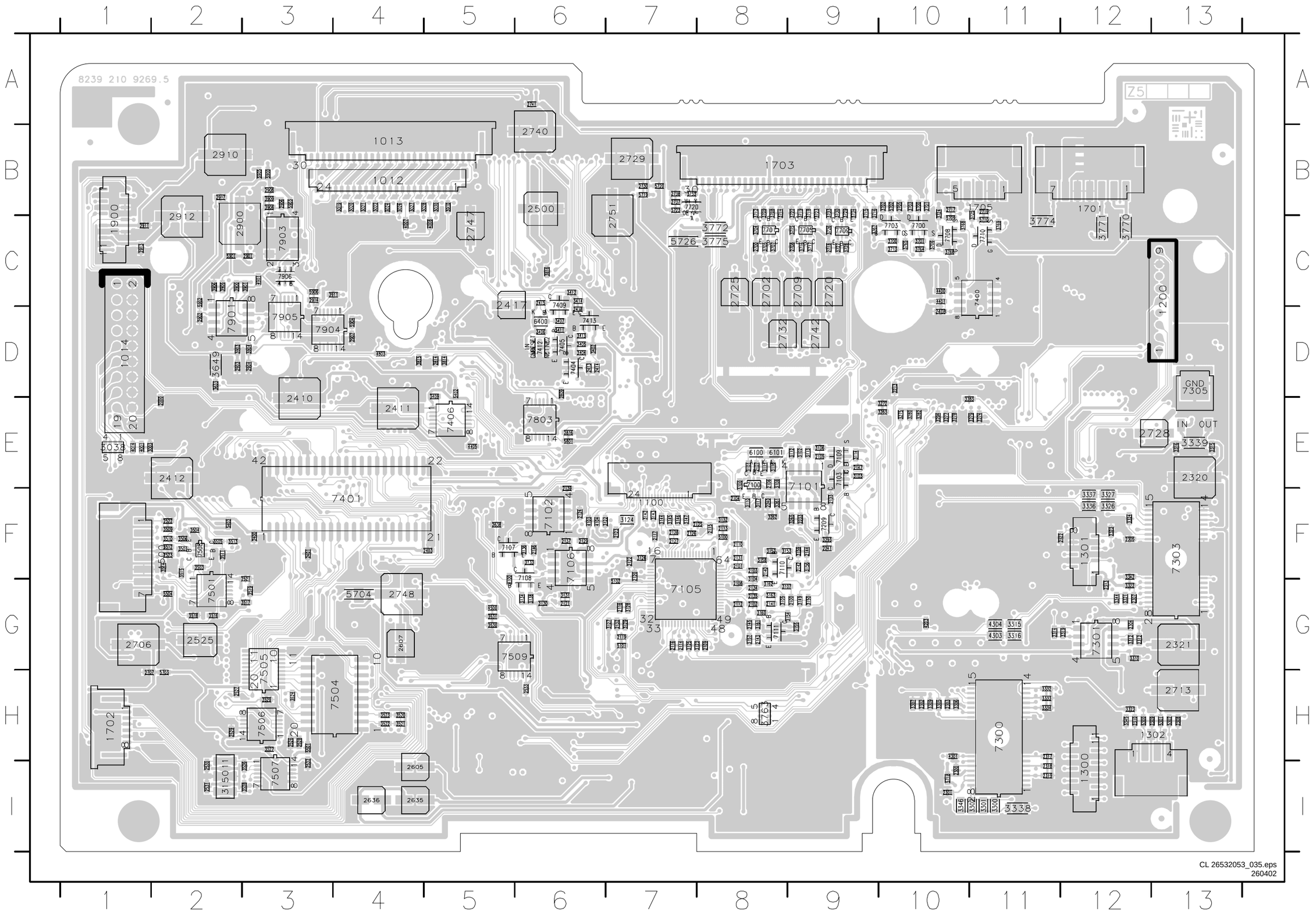
V DC Vtg measured in STOP MODE

BARE BOARD : 3139 243 34065

CL 26532053_034.eps 260402

1012 E17
1013 K16
1014 B2
2000 E2
2004 F14
2005 G14
2006 G14
2007 H8
2008 H14
2009 H14
2010 I14
2011 I14
2012 J14
2013 J14
2014 E14
2015 E14
3003 E4
3008 C4
3010 B4
3019 F12
3020 G12
3021 G12
3022 H12
3023 H3
3024 H12
3025 H6
3026 I12
3027 I12
3028 J12
3029 J3
3030 J12
3031 J6
3032 J7
3033 I3
3034 D12
3035 E12
3036 A4
3037-A B3
3037-B B3
3037-C C3
3037-D D3
3038-A D3
3038-B C3
3038-C C3
3038-D B3
4001 D3
4005 H5
4006 K5
4007 H12
4008 I12
4014 E3
7000-A H4
7000-B J4
7000-C H8
7000-D J8
F013 K1
F014 K1
F015 F12
F016 F13
F017 G5
F018 G12
F019 G13
F020 G12
F021 G13
F022 H3
F023 G9
F024 H12
F025 H13
F026 H12
F027 H13
F028 I12
F029 I13
F030 E14
F031 I12
F032 I13
F033 J12
F034 J13
F035 J12
F036 J3
F037 D14
F038 D14
F039 D14
F040 D14
F041 K3
F042 K12
F043 K6
F044 J13
F060 D3

Top Side



CL 26532053_035.eps
260402

Mapping Top Side

1012	B4	2321	G13	3024	B4	3319	G12	3730	B9	7106	F6		
1013	B4	2322	F12	3026	B4	3321	G12	3733	B9	7107	F5		
1014	D1	2323	F12	3027	B4	3322	G12	3734	B9	7108	F6		
1100	F7	2400	F3	3028	B4	3323	H12	3753	B7	7109	E9		
1200	C13	2401	F3	3030	B5	3324	F12	3763	H8	7110	F8		
1300	I12	2403	F5	3038	E1	3326	F12	3764	C10	7111	G8		
1301	F12	2408	D10	3100	E8	3327	F12	3765	C10	7209	F9		
1302	H13	2410	E3	3101	E8	3332	H11	3766	C10	7300	H11		
1500	F2	2411	E4	3102	E9	3333	H11	3767	C9	7301	G12		
1501	I2	2412	E2	3103	E9	3334	H11	3768	C10	7303	F13		
1701	B12	2413	D6	3104	F8	3336	F12	3769	C11	7305	D13		
1702	H1	2414	D6	3105	G8	3337	F12	3770	C12	7400	C11		
1703	B8	2415	C6	3106	E9	3338	I11	3771	C12	7401	F4		
1705	B11	2417	C5	3107	G8	3339	E13	3772	C8	7404	D6		
1900	C1	2418	D6	3108	E8	3342	F12	3774	C11	7405	D6		
2000	E2	2500	B6	3110	F8	3344	G12	3775	C8	7406	E5		
2100	G9	2521	F3	3111	E8	3345	H12	3814	D5	7409	C6		
2101	F8	2522	F2	3112	E9	3346	I10	3815	D4	7412	D6		
2102	G8	2523	F2	3113	E9	3402	D6	3816	C6	7413	D6		
2103	F8	2525	G2	3114	E9	3404	D6	3900	C2	7501	G2		
2104	F8	2526	H3	3116	E8	3405	D6	3901	C3	7504	H4		
2105	E9	2527	H2	3117	F8	3406	D6	3903	D2	7505	G3		
2106	E8	2528	H3	3122	F6	3407	D6	3904	D3	7506	H3		
2107	E8	2529	H2	3123	G8	3409	D5	3905	C2	7507	I3		
2108	G8	2530	I2	3124	F7	3411	D6	3906	C2	7508	F2		
2109	G8	2531	I2	3125	G7	3412	C6	3908	B3	7509	G5		
2110	F8	2532	I3	3126	F7	3413	D6	3909	B3	7700	C10		
2112	G8	2533	H6	3127	G7	3414	C6	3910	B5	7701	C8		
2113	F8	2605	I4	3128	G7	3501	F2	3911	C4	7703	C10		
2114	G7	2607	G4	3129	G7	3503	F2	4001	E1	7705	C9		
2115	F8	2635	I4	3130	G6	3504	F2	4007	C4	7708	C10		
2116	G7	2636	I4	3131	G6	3505	F2	4008	C5	7709	C9		
2117	F7	2638	F5	3132	F8	3506	F2	4014	E1	7710	C11		
2118	G7	2700	C8	3133	F6	3509	F2	4100	G5	7720	B7		
2119	G7	2701	B10	3134	G6	3510	F2	4103	F6	7803	E6		
2120	F7	2702	C8	3136	F6	3511	F2	4104	F6	7901	D2		
2121	G6	2705	B10	3138	G6	3512	F2	4203	G10	7903	C3		
2122	F7	2706	G1	3142	F7	3513	F2	4301	H10	7904	D3		
2123	F7	2707	H1	3143	F7	3514	F2	4303	G11	7905	D3		
2124	F6	2708	C9	3144	F7	3515	F2	4304	G11	7906	C3		
2125	F8	2709	C9	3145	F7	3516	G2	4400	C10				
2126	F7	2713	H13	3146	F7	3517	G3	4401	C10				
2127	F7	2715	B9	3147	F7	3518	G2	4405	E5				
2128	F7	2716	B9	3149	G9	3519	G3	4500	G5				
2129	F6	2717	B10	3150	G9	3520	H4	4803	D4				
2131	F8	2718	C9	3152	F8	3521	H4	4901	C3				
2132	G7	2719	B11	3153	F8	3522	H4	5100	F8				
2133	F9	2720	C9	3154	G9	3523	H4	5101	G7				
2134	G8	2725	C8	3155	G9	3524	H3	5102	G7				
2135	G8	2728	E13	3156	F9	3526	I3	5300	H12				
2137	F6	2729	B7	3157	G8	3527	H3	5301	H13				
2139	F6	2730	B7	3158	F8	3528	I3	5302	H13				
2140	F8	2732	D8	3159	F9	3529	H3	5402	D5				
2141	G8	2737	B7	3160	G8	3530	G5	5403	F2				
2142	F9	2738	B7	3161	G8	3531	G5	5501	H3				
2143	G8	2740	B6	3162	G8	3633	D2	5504	G2				
2144	F9	2741	A6	3163	G8	3649	D2	5700	B10				
2145	G8	2742	D9	3261	F8	3700	C10	5702	B10				
2146	F6	2747	C5	3262	F8	3701	C10	5703	H2				
2147	E9	2748	G4	3263	E10	3702	B10	5704	G4				
2213	D10	2751	C7	3265	F9	3703	B10	5709	C10				
2233	F9	2809	D6	3272	E10	3704	C8	5710	C11				
2240	F8	2814	D5	3274	E11	3705	C8	5718	I10				
2241	F9	2816	E6	3275	E10	3706	C10	5719	B7				
2300	I10	2900	C2	3277	E10	3707	C8	5720	B7				
2301	I10	2901	C3	3278	E10	3708	B8	5723	B7				
2302	H10	2902	D2	3279	E11	3709	B8	5726	C7				
2303	H10	2903	D2	3280	E10	3712	B8	5801	E6				
2304	G12	2904	D3	3282	E10	3713	C10	5900	B3				
2305	F12	2906	B3	3283	E10	3714	B8	5901	C2				
2307	G12	2907	D4	3293	F9	3715	C9	5902	C2				
2308	H13	2908	B3	3294	E10	3716	C9	5903	B3				
2309	H13	2910	B2	3300	I11	3717	C9	5904	D4				
2310	H12	2911	C1	3301	I11	3718	B9	5905	B3				
2312	G12	2912	C2	3302	I11	3719	B9	5906	C3				
2313	G12	2913	C1	3305	H10	3722	B9	6100	E8				
2314	G11	2914	C3	3306	H10	3723	B9	6101	E8				
2315	E13	2917	B2	3307	H10	3724	B10	6400	D6				
2316	E13	3003	E1	3309	H10	3725	B11	7100	E8				
2317	H11	3019	B4	3310	G12	3726	C9	7101	E9				
2318	I11	3020	B4	3312	G12	3727	C9	7102	F6				
2319	I11	3021	B4	3315	G11	3728	C9	7103	E9				
2320	E13	3022	B4	3316	G11	3729	B9	7105	G7				

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Mapping Bottom Side

2004	B10	2619	F7	3207	F2	3623	F7	4602	G10				
2005	B10	2620	G7	3208	G3	3624	G10	4605	F7				
2006	B10	2621	H9	3209	G3	3625	F7	4606	F7				
2007	B11	2622	H10	3210	G3	3626	G10	4800	E8				
2008	B10	2623	F10	3211	G3	3627	G10	5200	G2				
2009	B10	2624	E9	3212	G4	3628	F10	5201	G3				
2010	B10	2625	E9	3213	G4	3629	G10	5202	E6				
2011	B10	2626	G7	3214	F1	3630	G10	5203	C2				
2012	B9	2627	F7	3215	G4	3631	H7	5204	C2				
2013	B9	2628	H8	3216	G4	3632	H8	5401	D11				
2014	B10	2629	H9	3217	G4	3634	H8	5502	C7				
2015	B11	2630	G10	3218	G4	3635	H7	5505	G12				
2200	G3	2631	F10	3219	F2	3636	H7	5600	G10				
2201	G4	2632	E9	3221	G4	3638	H10	5601	H7				
2202	D3	2633	E8	3222	G4	3642	G7	5602	F7				
2203	D4	2634	F7	3223	G4	3643	G6	5603	G7				
2204	G4	2637	G7	3224	G4	3644	G11	5701	G6				
2205	G3	2703	G7	3225	E2	3645	G7	5705	I6				
2206	F3	2704	G6	3226	F2	3646	G6	5706	F6				
2207	G3	2710	I6	3227	G4	3647	H9	5707	I6				
2208	F5	2711	F7	3228	G4	3648	E8	5708	H6				
2209	D3	2712	F6	3229	G4	3710	G7	5712	F6				
2210	F3	2714	H6	3233	E1	3711	G6	5713	D7				
2211	E2	2721	F7	3234	E1	3720	F7	5714	D7				
2212	E2	2722	F6	3235	G4	3721	F6	5715	H6				
2214	D3	2723	D7	3236	F2	3731	F7	5716	F1				
2215	G4	2724	C6	3237	F2	3732	F6	5717	E1				
2216	F2	2726	H6	3238	E1	3735	C6	5721	C7				
2217	G5	2727	H6	3239	F2	3736	C6	5722	H6				
2218	F2	2731	C5	3240	E1	3737	C6	5724	G6				
2219	F5	2733	H6	3241	F2	3738	B6	5725	I6				
2220	F5	2734	H6	3242	G5	3739	B6	5800	E7				
2221	C3	2735	B7	3243	E1	3740	H6	5802	E7				
2222	E2	2736	C7	3244	E1	3741	H6	6300	I3				
2223	E2	2739	C5	3245	G2	3742	B6	6301	I3				
2224	E2	2743	G6	3246	F2	3743	B6	6302	I4				
2225	E2	2744	G6	3247	F5	3744	C5	7000	B11				
2226	E2	2745	F1	3250	E5	3745	C5	7200	E2				
2227	E5	2746	E1	3251	C3	3746	C6	7201	F2				
2228	E5	2749	D7	3252	E2	3747	B5	7202	F2				
2229	E5	2750	D7	3255	E5	3748	B5	7203	E1				
2230	E5	2800	E9	3256	E2	3749	H6	7204	E2				
2231	E5	2801	D9	3257	E2	3750	H6	7207	E4				
2232	E5	2802	E8	3266	C3	3751	B5	7208	D2				
2234	D6	2803	D7	3267	D6	3752	B6	7402	E11				
2235	D5	2804	D7	3268	D5	3754	C5	7403	F12				
2236	D5	2805	C8	3270	D5	3755	C5	7500	H11				
2237	D5	2806	C8	3271	D5	3756	C5	7502	B8				
2238	D5	2807	E8	3273	D5	3757	B5	7601	G9				
2239	E5	2808	C8	3284	E5	3758	B5	7704	I6				
2306	F1	2810	D9	3287	E5	3759	G6	7707	H6				
2311	F2	2811	E9	3288	E1	3760	G6	7713	D7				
2402	E12	2812	E9	3289	E2	3761	B5	7714	C6				
2405	D11	2813	E9	3290	E2	3762	B5	7716	D1				
2501	C9	2815	E7	3291	E1	3773	B6	7717	C5				
2504	C7	2817	C9	3304	I2	3800	E8	7719	C7				
2505	H11	2915	C12	3308	H2	3801	E10	7721	C5				
2506	G12	2916	C12	3313	F2	3802	D10	7800	D8				
2507	C8	2918	B12	3317	G2	3803	E9	7801	E9				
2510	C8	2919	C11	3325	F2	3804	E9	7802	E8				
2511	H12	3008	C12	3328	F2	3805	E9	7902	C11				
2512	H11	3010	D12	3340	G2	3806	E9						
2513	C8	3023	B11	3341	G1	3807	D9						
2516	B8	3025	B11	3343	G2	3808	E8						
2517	B8	3029	C11	3401	D11	3809	E8						
2518	G11	3031	B11	3403	E12	3810	E7						
2519	H11	3032	C11	3502	H12	3811	E7						
2520	G11	3033	B11	3507	B8	3812	D9						
2524	G12	3034	B11	3508	C8	3813	D9						
2601	E7	3035	B10	3600	H7	3902	C11						
2603	G10	3036	C12	3604	E9	3907	C12						
2604	H10	3037	C12	3605	E9	3912	C12						
2606	G7	3118	E5	3606	G10	3913	B12						
2608	G10	3119	E6	3607	G10	3914	D12						
2609	H7	3120	E5	3608	G10	3915	D11						
2610	H8	3121	E5	3609	H8	3916	D12						
2612	H8	3200	G3	3611	E8	4005	B11						
2613	H7	3201	G3	3612	E8	4006	B11						
2614	H7	3202	E2	3613	E8	4200	C3						
2615	H10	3203	G3	3614	G10	4201	D3						
2616	H10	3204	G3	3616	H7	4204	E2						

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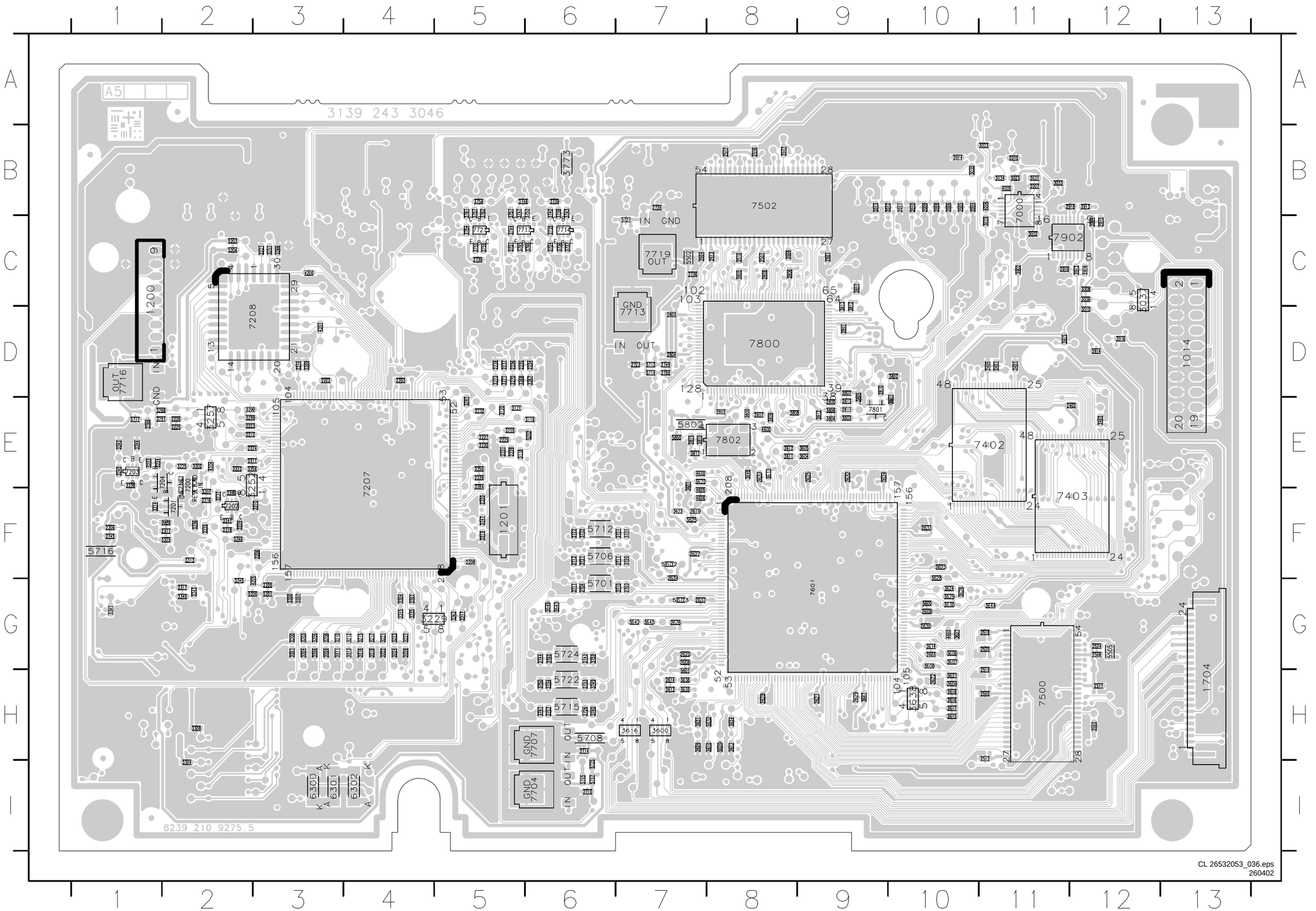
Bottom Side


A5
3139 243 3046
8239 210 9275.5
7208
7207
7502
7719 OUT
GND 7713
IN OUT
7800
7902
7000
7402
7403
7601
7500
7802
1200
1201
1704
1014
7716
5716
5712
5706
5701
5724
5722
5715
5708
GND 7707
GND 7704
6300
6301
6302
3616
3600
5802
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Personal Notes:

Personal Notes:

8. Alignments

Not applicable.

9. Circuit Descriptions, List of Abbreviations and IC Data

Index of this chapter:
1. Introduction
2. Loader/Mono Board
3. Abbreviations
4. IC Data

Notes:
- Only the new circuit parts are described. For the other descriptions, see the SD4.0 Service Manual (3122 785 12240).
- For a good understanding of the following circuit descriptions, please also check the diagrams in chapter 6 and 7.

9.1 Introduction

9.1.1 Features

The SD4.0SA_CH modules consist of the Mercury 3 Loader VAL6013/01 (from Philips Optical Storage), and a Mono Board. The module is capable of analogue video (with option for digital YUV video) and digital audio and SACD decoding.

9.1.2 Differences

The DVD-module SD4.0SA_CH is based on its predecessor the SD4.0, with similar functional block partitioning. However, the implementation of most functional blocks has been redesigned due to a new:
- Furore IC for SACD decoding.
- Module interface.
- Mechanical construction.

9.1.3 Modules

The main modules are:
- Mercury 3 Loader - VAL6013/01.
- Mono Board.

9.2 Loader/Mono Board

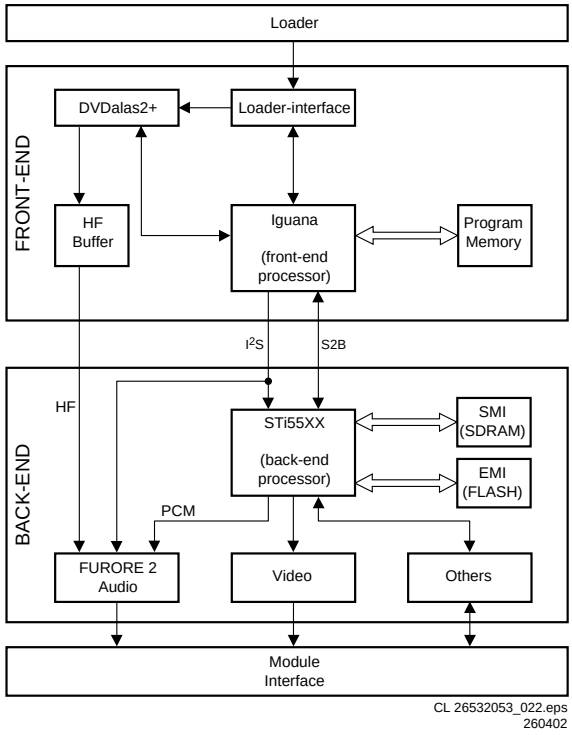

Figure 9-1 Block Diagram Loader/Mono board

The SD4.00_SA_CH (SACHI_4) is the 2nd generation Philips Architectural Standard Design of SACD mono board based on Furore 2, and will be used in the new generation of SACD players. It is designed in a multi-task way so that it can support the following optional main functions:
- SD4.00_SA_CH: Support SACD player with 5-disc changer.
- SD4.00_SA: Support SACD player with single-disc.
- SD4.00_CH: Support DVD player with 5-disc changer but without SACD playback.
- SD4.00_SA_I2C: Support SACD player with single-disc and I2C slave.

The SD4.00_SA_CH (SACHI_4) module consist of the following key components:
1. OPU: Mercury 2 Loader VAL6011/14 (slim type) for a single-disc SACD player, or DVD VAM6001/14 mechanism for a 5-disc SACD changer.
2. **Front-end:** M2 Basic Engine.
3. **Back-end:** DVD Host Processor STi55xx and Furore 2 SACD DSD/DST decoder.
4. **Power supply:** To convert the PSU voltages to the correct values.
5. **Reset circuit:** This circuit that the booting of the several devices on the mono board takes place in the correct order.

9.2.1 The Optical Pick-up Unit (OPU)

The Mercury 2 Loader has an optical unit consisting of two lasers:

- One for CD with a wavelength of 780 nm.
- One for DVD with a wavelength of 650 nm.

The TZA1033 (item 7105) controls the data from these lasers, and the supply to them.

9.2.2 Front-end: the Servo Part

The front-end consists of:
- The Loader interface
- The Servo Processor/Decoder
- The Interface/Program Memory

The Loader Interface

The TZA1033HL/K2 (or DVDALAS2plus, item 7105) is an analogue pre-processor and laser supply circuit. It contains data amplifiers and several options for radial tracking and focus control.
It is possible to optimise the dynamic range of this pre-amp/processor combination for the LF servo and RF data paths. The gain in both channels is separately programmable. This will guarantee an optimal playability for all kind of discs.
Also, a dual laser supply is implemented, with fully automatic laser control including stabilisation and an ON/OFF switch, plus a separate supply pin for power efficiency.

The Servo Processor/Decoder

In the SD3.0 module, the servo signals were fed to the MACE2 servo processor, while the HF output signal was fed to the SAA7335 decoder. In the new SD4.0SA_CH module, these ICs are combined into one chip: the SAA7812 Iguana.
This chip contains the following blocks: channel decoder, block decoder, servo processor, and microcontroller.
The servo circuit in the SAA7812 (item 7207) takes care of the servo controls.
In a CD system, there are some twelve control loops active. About six of them are needed to adjust the servo error signals that is once per disc rotation. It also adjusts offsets, signal amplitudes, and loop gains (AGCs), to enlarge system robustness and to avoid expensive potentiometer adjustments in production.
The other six loops determine the laser spot position on the disc in the radial, axial (focus), and tangential directions.
It also has to take care that the spot accesses a required position as fast as possible. This access system consists of two parts, namely the actuator and the sled, which are (within a certain range) mechanically and electrically independent. Therefore, during an access, the servo has to control as well the actuator as the sled.
The analogue signals, from the diode pre-processor, are converted into a digital representation using A/D converters.
For the communication between the host processor (STi55xx) and the servo processor, the S2B bus is used. This bus supports full-duplex asynchronous communication.

The SAA7812 is also a combined CD/DVD compatible decoding device. The device operates with built in hardware for CD/DVD error correction and de-interleaving operations. It decodes EFM or EFM+HF signals directly from the laser pre-amplifier, including analogue front-end, PLL data recovery, demodulation, and error correction.

Its analogue front-end input (the channel decoder), converts the HF input signal to the digital domain via an 8-bit ADC, preceded by an AGC circuit to obtain the optimum performance from the converter. An external resonator clocks this block.
This subsystem recovers the data from the channel stream. It corrects asymmetry, performs noise filtering and equalisation, and finally recovers the bit clock and data from the channel using a digital PLL.
The demodulator part detects the frame synchronisation signals and decodes the EFM (14 bit) and EFM+ (16 bit) data and sub-code words into 8-bit symbols. Via the serial output interface, the I^2S data (audio and video) go to the DVD decoder STi55xx.

The spindle-motor interface provides both motor control signals from the demodulator and, in addition, contains a tachometer loop that accepts tachometer pulses from the motor unit. They drive the motor IC (BA6665FM, item 7300).

The SAA7812 has two independent microcontroller interfaces. The first is a serial I^2C-bus and the second is a standard 8-bit multiplexed parallel interface. Both of these interfaces provide access to 32 8-bit registers for control and status.

The Interface/Program Memory

The interface between front-end (SAA7812) and back-end (Sti55xx) is via:
- I2S bus (BCLK, DATA, WCLK, FLAG, SYNC and V4).
- S2B bus (RXD_S2B, TXD_S2B, CPR_S2B and SUR_S2B).
- Miscellaneous I/O ports (RSTNF= front-end reset, EANF= front-end processor boot select).

Service tip: These lines contain series resistors (47 or 100 Ω) for easy hardware debugging, and for EMC/noise reduction of the high-speed I2S lines.

The front-end processor SAA7812 (Iguana) has two boot modes: normal boot from flash memory, or serial mode.
The boot selection is via the EANF pin. The Iguana samples the EANF signal level once during boot-up. Once boot-up is completed, this pin is no longer used for this purpose. However, in the SD4.0SA_CH circuit, the EANF is also connected to the flash memory. Therefore, when this pin is LOW, the lower 1Mbits of the memory is accessible. Conversely, when this pin is HIGH, the upper 1Mbits is accessible.
Under front-end normal operation, the program memory (less than 1Mbits in size) should reside in the lower bank. Therefore, the EANF pin should be LOW at all times. Since the actual flash memory used is 2Mbits, the upper 1Mbits is unused. This area is reserved for possible use by the front-end self-diagnostic software, or flash download application.

9.2.3 Back-end: the Digital Part

The back-end consists of:
- DVD back-end processor
- SACD DSD processor
- Audio output
- Video output
- Clock factory
- Miscellaneous

DVD Back-end Processor

The SD4.0SA_CH is designed for the Sti55xx family. Some of the DVD related features of these ICs are:

Processor overview

Function	STi5580	STi5588	STi5519
Basic CD/VCD/DVD decoding	X	X	X
Extra 2-channel of I2S output (PCMDATA3)	X	X	
Karaoke	X	X	
DTS	X	X	
Audio post processing (equalizer, level meter, etc)		X	
DVD audio		X	
Progressive scan at analog video output		X	

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Figure 9-2 Processor overview

The STi5580 has the same architecture as the STi5508 (used in earlier DVD generations), and is pin-to-pin compatible.
It works on 3.3 V (VDD), and comprises the following functions:
- Video decoder, which supports MPEG1 and MPEG2.
- Audio decoder that supports AC-3, MPEG1, MPEG2, DTS, PCM, S/PDIF, and MP3.
- PAL/NTSC video encoder with simultaneously Y/C, CVBS, and RGB/YUV outputs.

- The video encoder supports Closed Caption and allows MacroVision 7.0/6.1.
- Full screen On Screen Display (OSD) generator.
- Three on-chip PLLs to generate all necessary clocks (as reference the 27 MHz video clock is used).

Input
Input data comes from the I2S-bus. The front-end interface of this device, accepts DVD, CD and CD-DA information.

Signal Processing
For video, the input data stream is decoded to the appropriate MPEG, Sub Picture, and OSD data streams, after which they are fed to the PAL/NTSC encoder. This cell will convert the digital MPEG/Sub Picture/OSD stream into a standard base band signal and into RGB components. It handles interlaced and non-interlaced data, can perform CC/TXT encoding, and allows MacroVision copy protection.

For audio, the processing cell is a fully compatible DTS, Dolby Digital (AC-3), MPEG1, MPEG2, PCM decoder, capable of decoding 5.1 and 2 channel streams.

Output
For video, six analogue output pins are available on which CVBS, S-VHS (Y/C), and RGB signals are present. They go, via a buffer, to connector 1703. As an option, a digital YUV output is available at connector 1704.

External Memory
The STi55xx family is capable of accessing external memory via three buses:

- **The enhanced memory interface (EMI).** This interface is configurable and can be used to access Flash, ROM, and various flavours of DRAM.
- **The shared memory interface (SMI).** The SMI is only used to access SDRAM. The SMI is connected to a 64Mbits (4M x 16bit) 7.5ns SDRAM (item 7500). The SDRAM has the following functions:
  - It is used by the MPEG video decoder as a frame buffer,
  - It holds the software and the variables used by it.
- **The I2C bus.** Via this bus, the NVRAM (or EEPROM) is accessible. This memory is used to store user settings, player settings, and region code. As the STi55xx I/O-lines are potentially unable handle 5V inputs, a voltage level shifter is foreseen for all I2C-busses. This circuit will isolate the STi55xx I2C ports (3.3V) from the system I2C bus (5V). See figure below.

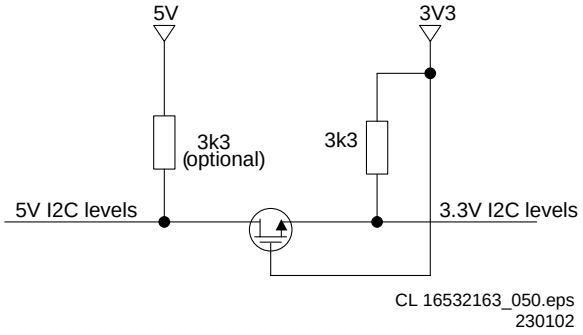

Figure 9-3 I2C voltage level shifter

The SACD DSD processor
The Furore-IC is a one-chip design, containing all the hardware that is required for SACD processing. It is intended to interface with the STixx-family DVD video decoders.
The Furore-IC contains a memory interface to support an external 16 or 64 Mbit SDRAM.
During SACD application, the STi55xx serves as a host, whereby the Furore is controlled via the EMI interface. The Furore processing part is not used during all other play modes. In these modes, the PCM audio signals are fed through the Furore to the appropriate DAC.

Block diagram

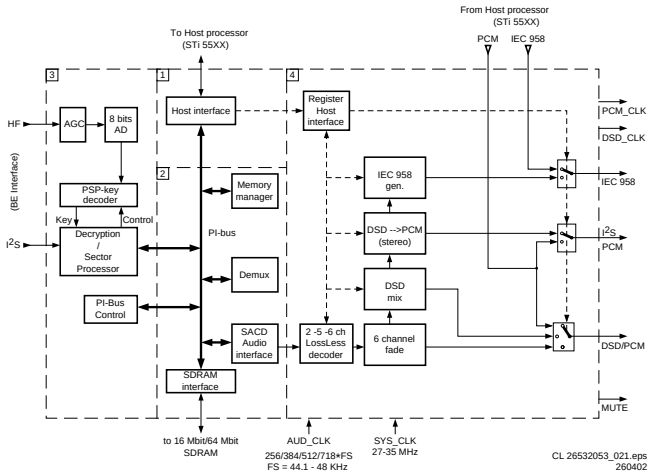

Figure 9-4 Block diagram Furore

We can divide the Furore-IC in four main parts (see block diagram):

1. **Host interface.** This is the link between the host bus and the internal registers and memory bus. It also supplies the general reset signal (HW and SW) and the interrupt signals.
2. **Data processing.** All modules and peripherals in this part are connected to a so-called PI-bus. It is beyond the scope of this manual to go more in detail on this subject.
3. **Copy protection.** On every SACD disc, a PSP-signal is recorded. The player can only play a disc if a valid PSP-signal is detected. This PSP-key is recorded, via a special mechanism, in the EFM-signal on the disc. To detect this key, the analogue HF-signal from the optical pick-up unit is fed directly to the Furore-IC. Via an AGC, the signal is fed to an ADC. The digitised HF signal is then fed to a block where key is encrypted. Control of this process is done via the host interface (sector processor).
4. **DSD decoding and post processing.** In this part, all processing is done to generate a DSD and/or an I^2S stream (from the de-multiplexed stream coming from the data processing block), in such a way that it can directly be connected to a DA-converter. All processing is done on 384*FS.

Interfaces

- **Basic Engine Interface:**
  - Data input interface. The Basic Engine Interface (I2S) is connected to the output of the SAA7335 (HD61) high speed CD decoder.
  - Analogue HF input. The analogue HF input, coming from the optical pickup unit (OPU), is also fed to the Furore-IC, to extract the copy-protection information PSP (Pit Signal Processing = invisible data is stored on to disc, which is required to decrypt the encrypted content).
- **SDRAM Interface:** The SDRAM interface forms a glue less interface to one 64 Mbit SDRAM device. The interface takes care for the power-up sequence, mode programming and refreshing of the SDRAM devices. This is hard coded in the interface and does not have to be controlled by the host.
- **Audio data input/output Interface:**
  - DSD/PCM combined data output. DSD_PCM: Output intended for a combined 6-channel DSD (SACD) and PCM (DVD-CDDA) DAC. Switching between the PCM data coming from the STi55xx, and the internal generated DSD signals, is done in the Furore IC.

- Stereo DSD only output. DSD_stereo: 2-channel DSD output with stereo down mix in the case of 5- and 6-channel, and normal stereo in case of 2-channel DSD mode.
- Stereo PCM data output. Two possible stereo sources can be selected as stereo PCM output:
  1. Stereo PCM coming from the STi55xx via the PCM input on Furore.
  2. Stereo or down-mix-PCM derived via a decimation filter from the SACD-DSD signal.
- Digital audio output interface (IEC958). The IEC958 format is intended to connect the DVD736SA to a digital receiver. No DSD signals are defined for IEC958, therefore the 'DSD-->PCM converted' signal is transmitted. Following two types of signals are possible on the digital interface:
  1. IEC958 data coming from the STi55xx.
  2. IEC958 data (stereo or down-mix-PCM) derived via a decimation filter from the SACD-DSD signal.
- Clock + reset input. Two different processing clocks and a reset pulse are needed:
  1. Sys_clk: System clock for data processing part, frequency can be 27 MHz or 768*FS.
  2. 384*FS: Processing clock for LLD and post processing.
  3. RESETn is an asynchronous reset and should be low for at least 1 period of DSD_CLK.

Memory

- SDRAM.
  - The size of the SDRAM is 64 Mbit.
  - The SDRAM (items 7500 and 7502) has the following functions:
  - It is used by the MPEG video decoder as a frame buffer,
  - It holds the software and the variables used by it.
- **Flash-ROM.** Two 2MB Flash-ROMs (items 7402 and 7403) hold the DVD firmware, and are controlled by pin 16 (FLASH_OEN) of the STi55xx. It must be able to perform a download (by disk or OS-link) in a Flash-only system.
- EEPROM. User settings, player settings, and region code are stored in a 32 Kb I^2C EEPROM.

Audio Output

The audio interfaces available in SD4.0SA_CH are I2S and S/PDIF for digital audio output, and I2S karaoke microphone input.
In SACD player, two types of DACs (that are PCM DAC and high end DSD DAC), are used on AV board.
The audio data path to both DACs is routed via the Furore 2.

I2S audio

The STi55xx is capable of 6-channel I2S output. These channels can be configured to output 5.1 Dolby Digital, DTS, etc.

- PCM_OUT0: Left and Right.
- PCM_OUT1: Centre and LFE (subwoofer).
- PCM_OUT2: Left and Right surround.

Two additional channels (available in STi5580 and STi5588) are capable of providing down-mixed stereo.

S/PDIF

The S/PDIF signal level (pin 57, SPDIF_OUT) is 5V TTL at module interface. To meet the complete S/PDIF specifications, an external de-coupling circuit (item 7720, diagram M7) is implemented.

I2S karaoke (optional)

The STi5580 and STi5588 have built-in karaoke processing. The internal karaoke block accepts I2S signal, acting as the master by generating the required KOKPCMCLK frequency. This frequency is always 1/4 the music sampling frequency.
An external analogue-to-digital converter (ADC), acting as slave, is required to convert the microphone signals to I2S signals.

CD-DA/DVD Data Path

The data path for CD-DA and DVD is as follows:

- I2S data from the M2 basic engine enters the STi55xx.
- The STi55xx processes the data, and sends the 6 PCM output channels to Furore 2. The LeRi channels are directly passed to the AV board also.
- The switch matrix of the Furore 2 sends the two incoming stereo PCM channels (LeRi) to the AV board.
- The switch matrix of the Furore 2 sends the six incoming PCM channels to the high end DAC board.
- The mute signal from the STti55xx is directly passed to the AV board. This requires a patch on the mono board.
- The IEC958 output of the STi55xx is fed directly to AV board.

The clock distribution is as follows:

- The master clock 384FS is received from the high end DAC board.
- From this clock the 27 MHz clock for STi5580 and the Furore 2 is derived (Video clock).
- From the 27 MHz clock the audio clock (256FS) is derived. The STi55xx and Furore 2 use this clock. For CD-DA FS amounts to 44.1 KHz, for DVD 48 or 96 KHz.
- In case of CD-DA, the high end DAC uses its internal clock (384FS). In case of DVD, the switch matrix of Furore 2 sends the audio clock (256FS) to the high end DAC on AV board.
- The AV board receives the 256FS clock.

Selection of the audio clock is done in the clock factory. For a description of the clock factory, see paragraph 'Clock Factory'.

SACD Data Path

The data path for DSD/DST is as follows:

- I2S data from the basic engine enters the Furore 2.
- The Furore 2 processes the data. This results in 6 DSD/DST channels.
- The switch matrix of the Furore 2 sends the 6 DSD/DST channels to the high end DAC on AV board.
- The 6 DSD/DST channels are down mixed to a stereo PCM signal.
- The switch matrix of the Furore 2 sends the stereo PCM signal to the AV board.
- The mute signal from the STi55xx is directly passed to the AV board. This requires a patch on the mono board.

The clock distribution is as follows:

- The master clock 384FS is received from the high end DAC on AV board.
- From this clock the 27 MHz clock for Sti55xx and Furore 2 is derived (video clock).
- From the 27 MHz clock the audio clock (256FS) is derived. The STti5580 and Furore 2 use this clock.
- The high end DAC on AV board uses its own XTAL clock (384FS). The 256FS clock to the DAC board is switched off, to prevent for interference.
- The AV board receives the 256FS clock.

Selection of the audio clock is done in the clock factory. For a description of the clock factory, see paragraph 'Clock Factory'.

Video Output

Digital video (optional)

Digital YUV output is routed directly from STi55xx ports to a 24-pin connector (item 1704). From the same connector, the HSYNC, VSYNC and 27MHZ_CLK signals are available. The digital YUV connector is the interface to external video processing devices; such as high quality progressive scan codex and high quality video DAC.

Analogue video
The STi55xx is capable of 6-channel analogue video. Three channels (pins 25, 26 and 27) are RGB or YUV format, while the other three channels (pins 32, 33 and 34) are Y, C, and CVBS.
A video output buffer (see diagram M7, e.g. item 7701 for R) is implemented: an 8MHz/16MHz selectable filter stage and a 75Ω drive stage.

Clock Factory
One clock factory is implemented to support all clocks required by the Furore 2. The various master clock, which depends on whether SACD is present, is used for SD4.00_SA_CH. The clock factory of SD4.00_SA_CH is showed in Figure 8-2.

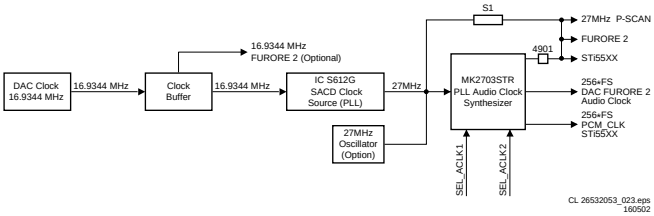

Figure 9-5 Block diagram clock factory

For the SACD player, the clock system is a DAC master clock system. For non-SACD player, the clock system is a mono board master clock system.
The Furore 2 supports clock 256*FS/384*FS/512*FS. The most convenient value in the market is 16.9344 MHz (384*FS, FS=44.1KHz). Therefore, the master clock on the SD4.00_SA_CH mono board is the 384*FS coming from the A/V board. The 384*FS (16.9344 MHz) from the DAC clock, must always be present. It is buffered before it is sent to the Furore 2 and the rest of the clock factory. The IC S612G delivers a 27 MHz system clock.
The Furore 2 and Sti5580/Sti5588 (Video) use this clock. It is used to derive the PCM audio clocks 256*FS by the MK2703STR. This IC is also used to buffer the incoming 27 MHz clock.
The communication between the Sti55xx and the Furore 2 is asynchronous.
To support non-SACD playback, an on-board 27MHz oscillator delivers the master clock for SD4.00_SA_CH mono board.

Miscellaneous
Most general IO ports are connected directly to the module interface. Compared with the SD3.0 module, some on-board circuits are removed, as it made more sense (and more cost effective) to implement these circuits externally.

SCART Status Signal
The SCART0 and SCART1 signals are directly available at the module interface, where the 0_6_12V signal is generated. See table below:

Table 9-1 0_6_12V SCART status truth table

Function	PIO3_6 (SCART0)	PIO3_7 (SCART1)	0_6_12V (at SCART connector)
TV display	1	1	0V
TV display	0	1	0V
16:9 aspect ratio	1	0	+6V
4:3 aspect ratio	0	0	+12V

Mute
The audio MUTE signal (active 'high') is directly available at the module interface.

Service

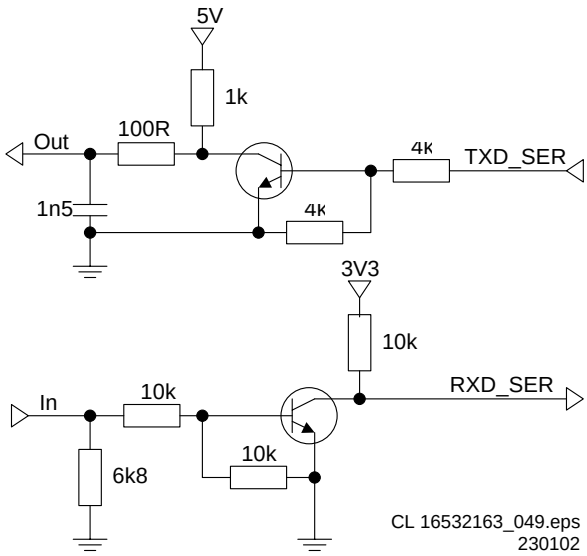

Figure 9-6 Service Port Buffer

The service port (see diagram M5) is simplified to reduce cost. The unused RTS and CTS lines are no longer connected. A transistor buffer (item 7508) is used instead of the Schmitt Trigger buffer (item 7501).
The overall loading and driving capability of the RS-232 emulator port is not greatly changed. However, as a precaution, the Schmitt Trigger circuit remains in the layout as an optional implementation.

This SD4.0SA_CH has the same ComPair connector as in previous DVD generations. Flashing of the application-SW is not possible with the ComPair cable, except with a CD-R disc. For sets with Mask-ROM software, replace it with a programmed Flash (available via your Philips Service organisation).

Power Supply (diagram M7)

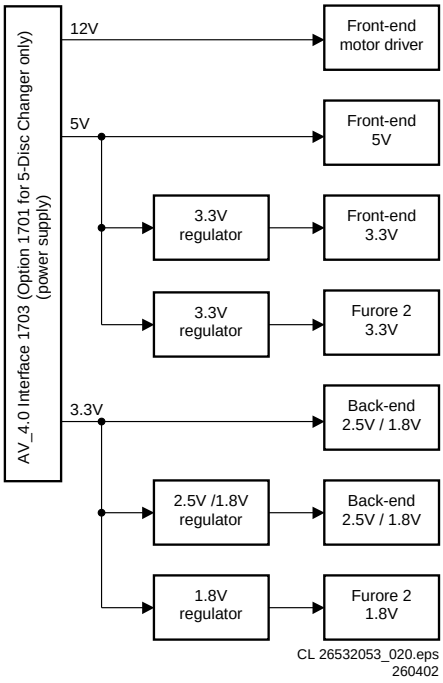

Figure 9-7 Mono Board Power Supply Block Diagram

The main power supplies to the module are 3.3V, 5V, and 12V (input via connector 1703).

The SACD DSD/DST decoder Furore 2 uses 1.8V for its core and analogue portion, and 3.3V for its interface. The on-board 1.8V linear regulator LF18ABDT and 3.3V linear LD1117DT33 are used to generate 1.8V and 3.3V power supply respectively. The back-end section mainly uses the 1.8V or 2.5V and 3.3V, which depend on which back-end processor is used. The on-board linear regulators LF25ABDT or LF18ABDT are used to generate the 2.5V (or 1.8V) required by the STi55xx.
The front-end section mainly uses the 5V and 12V. An on-board linear regulator LD1117DT33 can be used to generate the 3.3V required by the front-end. The 12V is used by the motor and servo drivers.

Reset Circuit

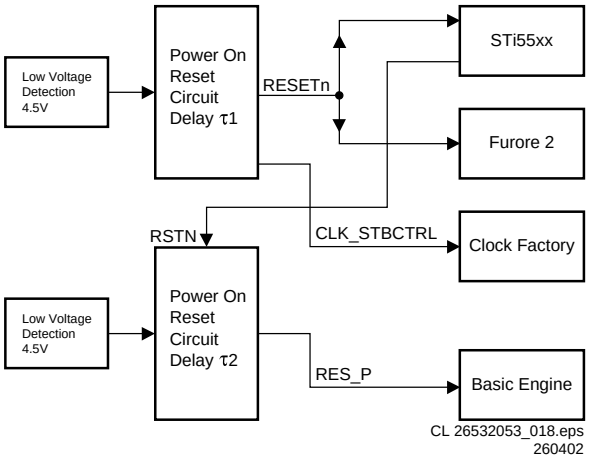

Figure 9-8 Block diagram of reset circuit

This reset circuit takes care that booting the different devices on the mono board takes place in the correct order. The correct reset order is:

1. The Power On Reset circuit (delay t1) creates a reset signal 'RESETn' to reset the STi55xx and Furore .
2. In the meantime, the Power On Reset circuit (delay t1) creates a reset signal 'CLK_STBCTRL', which is inverted to 'RESETn', to enable the Clock Factory.
3. Then, the Power On Reset circuit (delay t2) generates a reset signal 'RES_P' to reset the Basic Engine.
4. The STI55xx can now reset the Basic Engine via 'RSTN'.

9.3 Abbreviation List

ADC	Analogue to Digital Converter
AM	Amplitude Modulation
BE	Basic Engine
ComPair	Computer aided rePair
CD-DA	CD Digital Audio
CS	Chip Select
DAC	Digital to Analogue Converter
DAIO	Digital Audio Input Output
DENC	Digital Encoder
DFU	Direction For Use: description for the end user
DNR	Dynamic Noise Reduction
DRAM	Dynamic RAM
DSD	Direct Stream Digital
DSP	Digital Signal Processing
DTS	Digital Theatre Sound
DVD	Digital Versatile Disc
EEPROM	Electrically Erasable and Programmable Read Only Memory
EFM	Eight to Fourteen bit Modulation
EMI	External Memory Interface (STi55xx)
FFC	Flat Foil Cable
FLASH	Flash memory
HPF	High Pass Filter
HW	Hardware
I2C	Integrated IC bus (signals at 5V level)
I2S	Integrated IC Sound bus (signals at 3.3V level)
IC	Integrated Circuit
IF	Intermediate Frequency
IRQ	Interrupt Request
LLD	Loss Less Decoder
LPCM	Linear Pulse Code Modulation
LRCLK	Left/Right clock
LVTTL	Low Voltage Transistor Transistor Logic (3.3V logic)
MACE	Mini All Compact Disc Engine
MPEG	Motion Pictures Experts Group
NC	Not Connected
NVM	Non Volatile Memory: IC containing TV related data e.g. alignments
OC	Open Circuit
OPU	Optical Pick-up Unit
PCB	Printed Circuit Board (see PWB)
PCM	Pulse Code Modulation
PCM_CLK	Audio system clock for DAC
PCM_OUTx	Audio serial output data
PSU	Power Supply Unit
PWB	Printed Wiring Board (see PCB)
RAM	Random Access Memory
RGB	Red, Green and Blue colour space
ROM	Read Only Memory
S2B	Serial to Basic Engine, communication bus between host- and servo processor
SCL	Serial Clock I2C
SCLK	Audio serial bit clock
SDA	Serial Data I2C
SDRAM	Synchronous DRAM
S/PDIF	Sony Philips Digital InterFace
SRAM	Static RAM
STBY	Standby
SVCD	Super Video CD
SW	Software
THD	Total Harmonic Distortion
TTL	Transistor Transistor Logic (5V logic)
uP	Microprocessor
VCD	Video CD
Y/C	Luminance (Y) and Chrominance (C) signal
YUV	Component video

9.4 IC Data

In this paragraph, the internal blockdiagrams and pinning are given of ICs that are drawn as 'black box' in the electrical diagrams (with exception of 'memory' and 'logic' ICs).

9.4.1 Diagram M1

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply — TZA1033

DEVICE BLOCK DIAGRAM

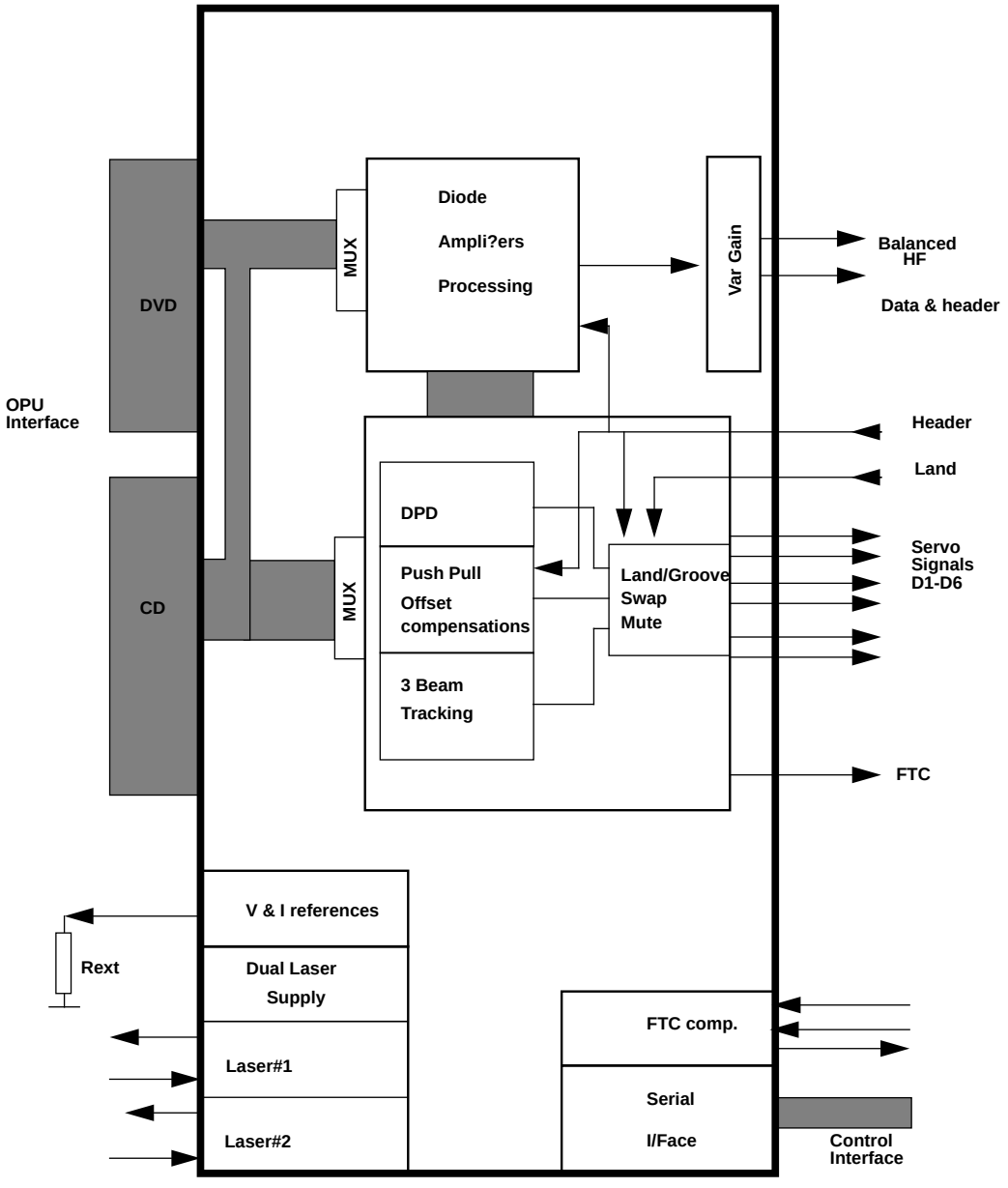

Figure 9-9 TZA1033 Device Block Diagram (item 7100)

DVDALAS2plus Advanced Analogue DVD Signal Processor and Laser Supply — TZA1033

PINNING

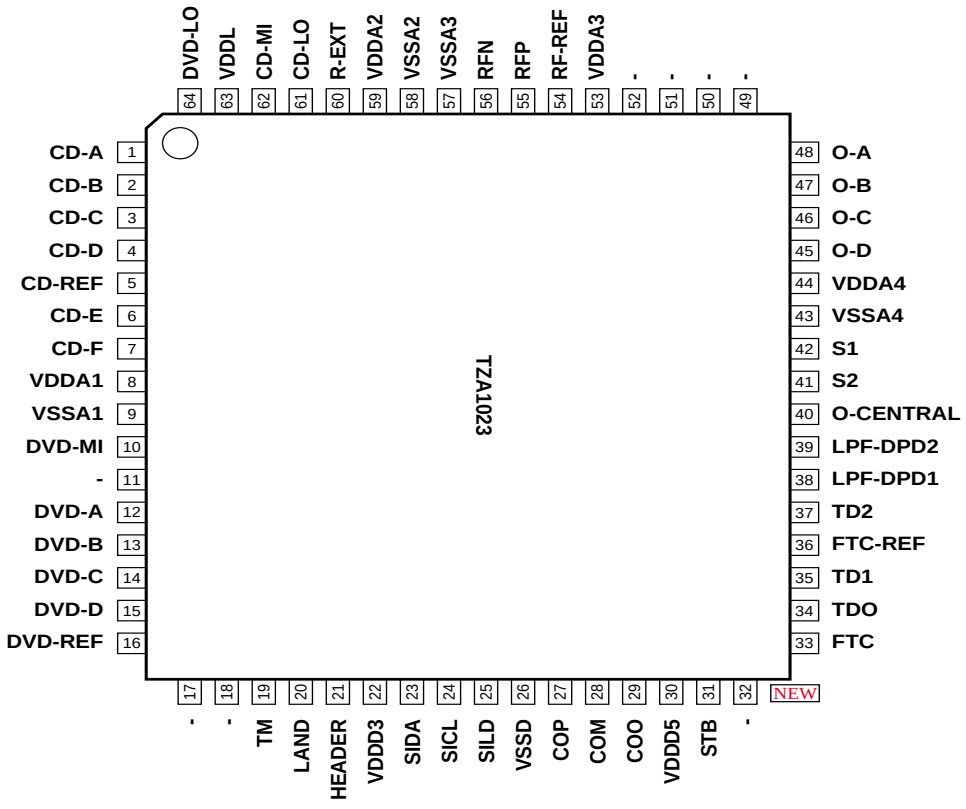

Fig.2 Pin configuration.

Figure 9-10 TZA1033 Pinning (item 7100)

9.4.2 Diagram M2

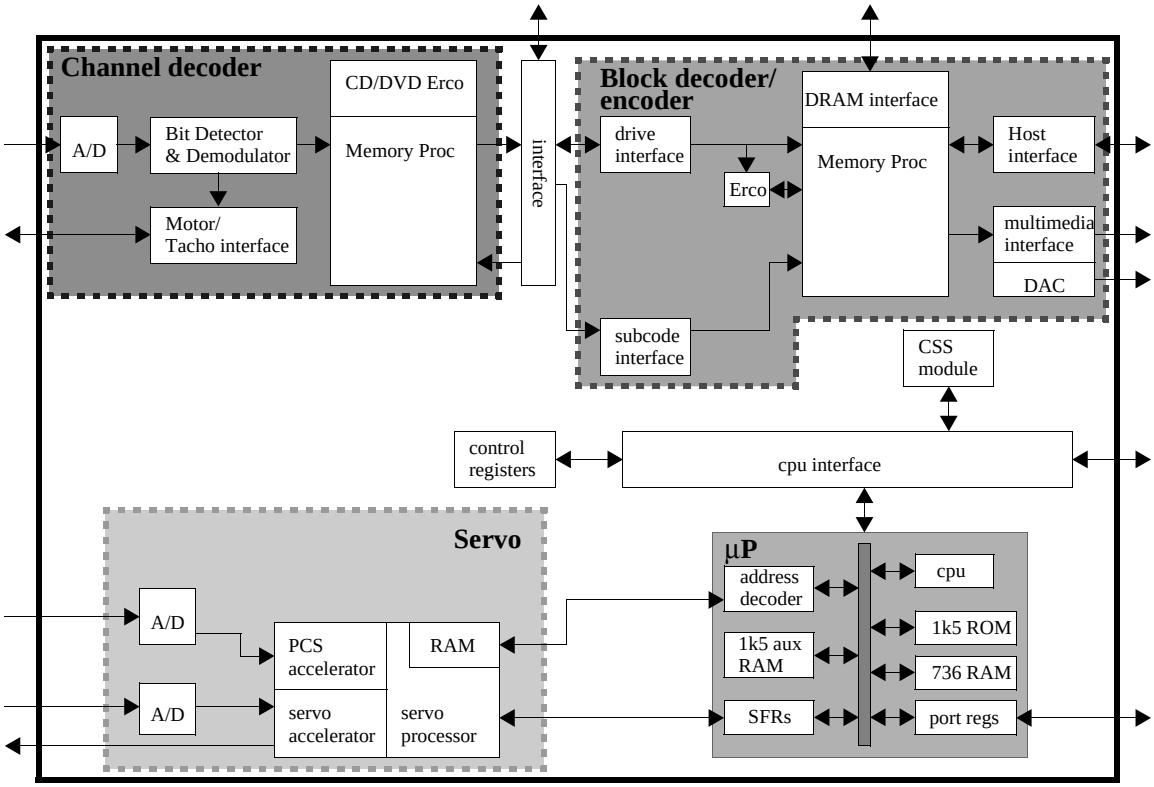

Figure 1 Functional Block Diagram

Figure 9-11 SAA7812HL Block Diagram (item 7200)

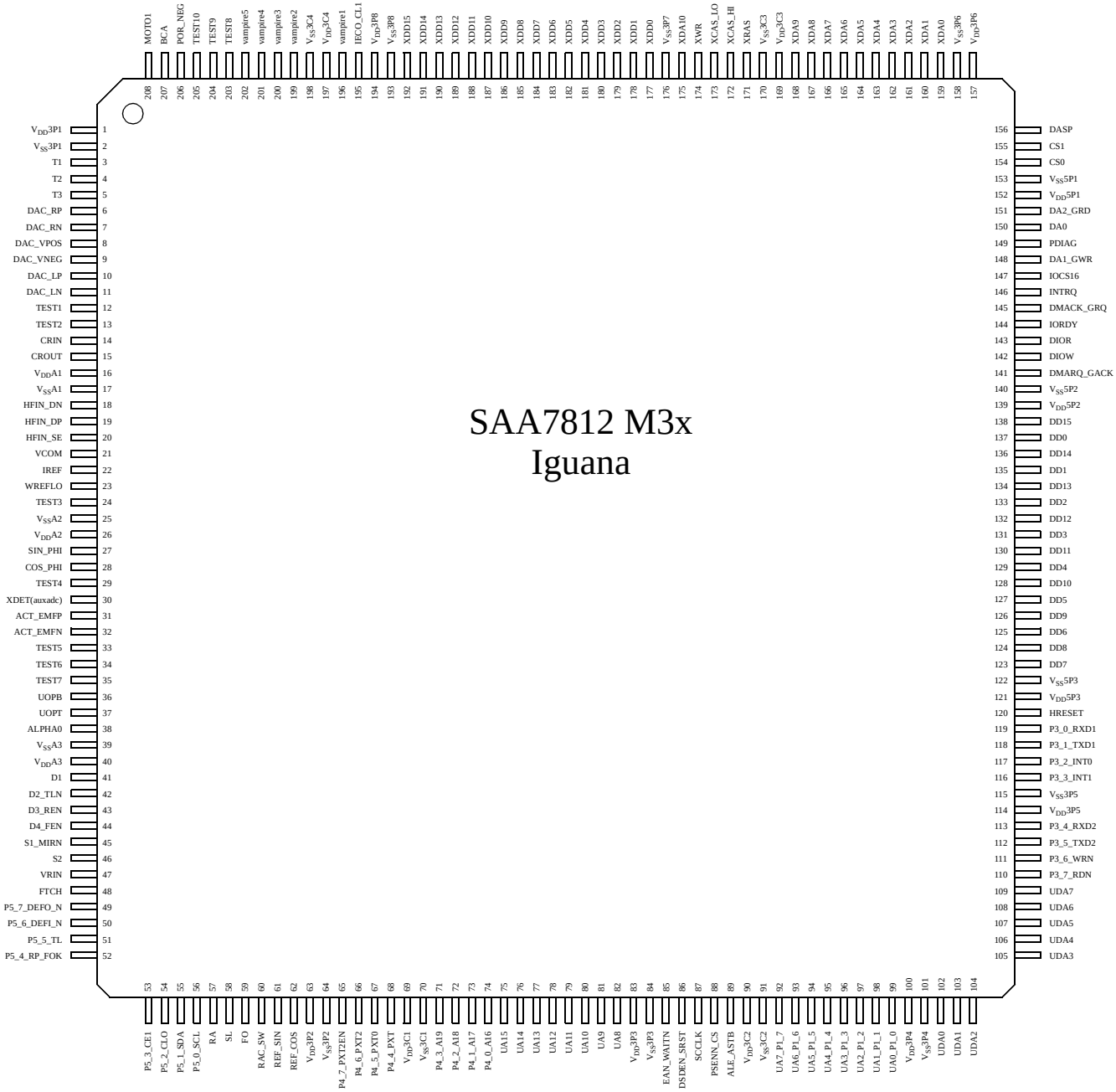

Figure 2 Pinning Diagram

Figure 9-12 SAA7812HL Pinning (item 7200)

9.4.3 Diagram M6

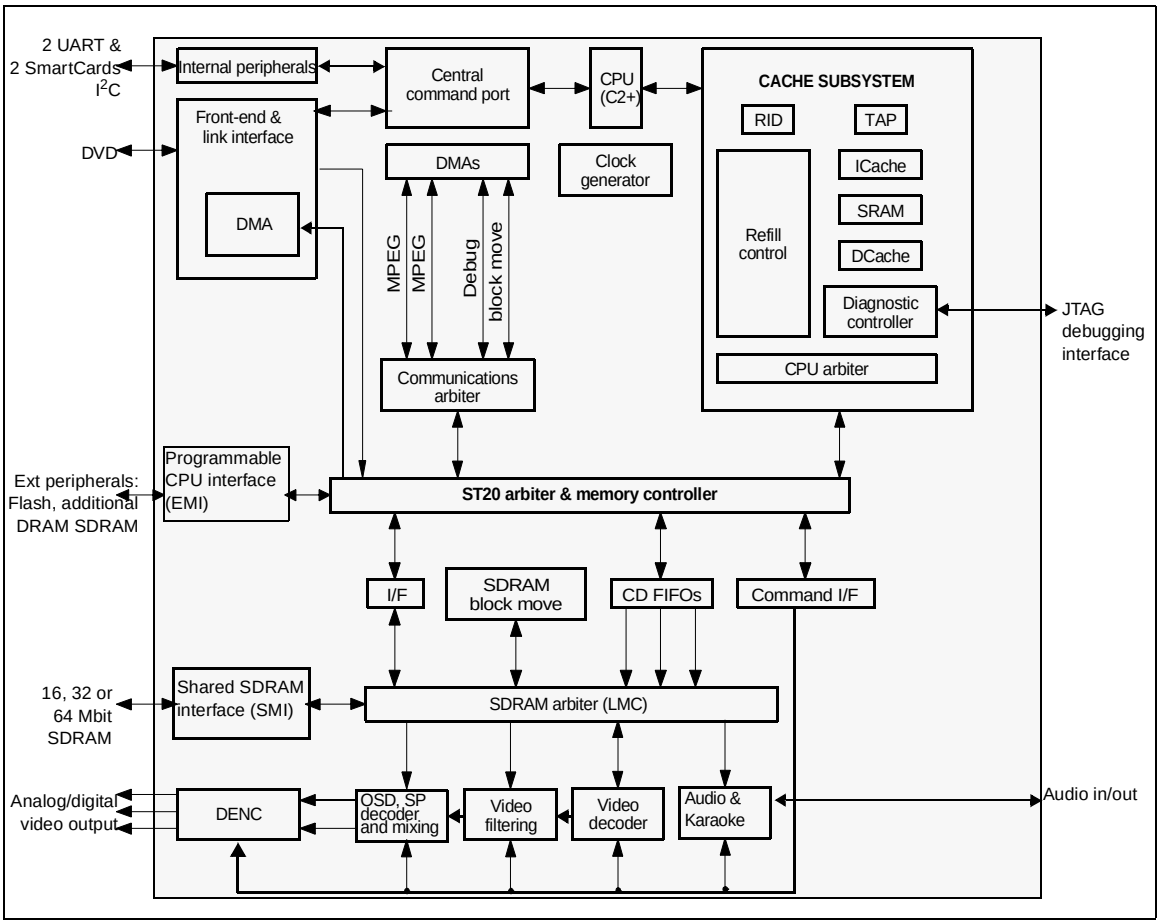

Figure 9-13 STi5580 Block Diagram (item 7600)

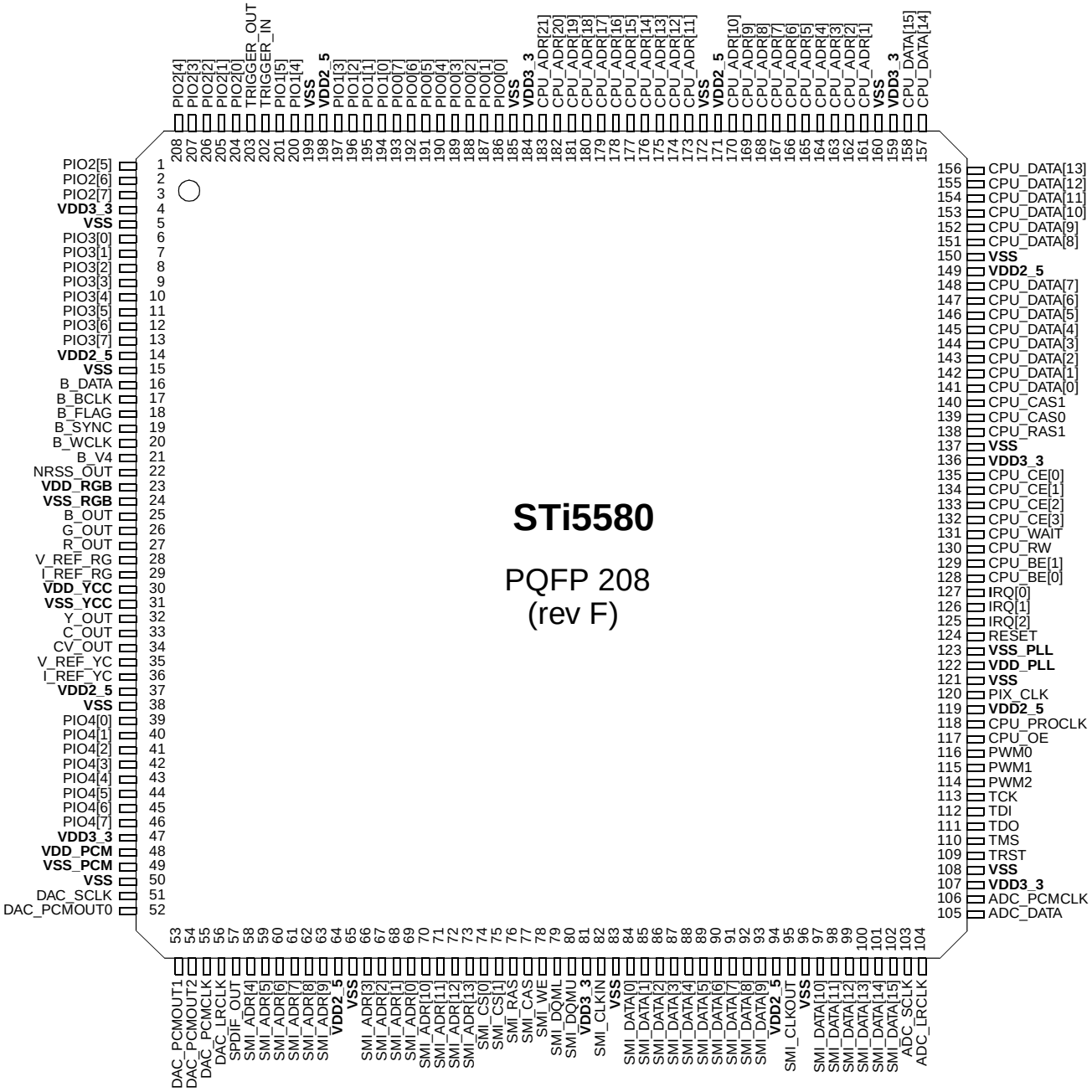

Figure 9-14 STi5580 Pinning (item 7600)

10. Spare parts list

Mono Board

Various

1013	2422 025 17451	CON BM H 30P F 1.00 FFC 0.3 R
1100	2422 025 17529	CON BM H 24P F 0.50 FFC 0.3 R
1201	2422 543 01292	RES XTL SM 8M4672 30P AT-41 R
1300	2422 025 17746	CON BM V 11P F 1.00 FFC 0.3 R
1301	2422 025 17747	CON BM V 8P F 1.00 FFC 0.3 R
1302	2422 025 16543	CON BM H 4P M 2.00 PH SMD R
1500	2422 025 16703	CON H 7P M 2.00 PH SMD R
1703	2422 025 17451	CON BM H 30P F 1.00 FFC 0.3 R

⊣⊢

2000	4822 126 13879	220nF 20% 16V
2100	4822 126 11785	0603 50V 47P PM5
2101	4822 126 13193	4.7nF 10% 63V
2102	2238 586 59812	0603 50V 100NP80M
2103	3198 016 31020	0603 25V 1nF
2104	2238 586 59812	0603 50V 100NP80M
2105	3198 017 41050	0603 10V 1µF COL R
2106	3198 017 36830	0603 16V 68nF COL
2107	3198 017 41050	0603 10V 1µF COL R
2108	2238 586 59812	0603 50V 100NP80M
2109	2238 586 59812	0603 50V 100NP80M
2110	3198 016 31020	0603 25V 1nF
2112	2238 586 59812	0603 50V 100NP80M
2113	2238 586 59812	0603 50V 100NP80M
2115	4822 126 13193	4.7nF 10% 63V
2117	4822 126 14494	22nF 10% 25V 0603
2118	4822 126 14507	18pF 5% 50V 0603
2119	2238 586 59812	0603 50V 100NP80M
2120	2238 586 59812	0603 50V 100NP80M
2121	4822 126 14494	22nF 10% 25V 0603
2122	2238 586 59812	0603 50V 100NP80M
2123	4822 126 13879	220nF 20% 16V
2124	2238 586 59812	0603 50V 100NP80M
2129	2238 586 59812	0603 50V 100NP80M
2131	2238 586 59812	0603 50V 100NP80M
2132	2238 586 59812	0603 50V 100NP80M
2133	2238 586 59812	0603 50V 100NP80M
2134	4822 051 30008	0R00 JUMPER
2135	4822 051 30008	0R00 JUMPER
2137	2238 586 59812	0603 50V 100NP80M
2139	4822 126 13879	220nF 20% 16V
2140	3198 016 36810	0603 25V 680P COL R
2141	3198 016 36810	0603 25V 680P COL R
2142	5322 126 11582	6.8nF 10% 63V
2143	5322 126 11582	6.8nF 10% 63V
2144	4822 126 14487	8.2pF 0.5% 50V 0603
2145	4822 126 14487	8.2pF 0.5% 50V 0603
2146	3198 016 31020	0603 25V 1nF
2147	5322 126 11583	10nF 10% 50V 0603
2200	2238 586 59812	0603 50V 100NP80M
2201	2238 586 59812	0603 50V 100NP80M
2202	2238 586 59812	0603 50V 100NP80M
2203	2238 586 59812	0603 50V 100NP80M
2204	2238 586 59812	0603 50V 100NP80M
2205	2238 586 59812	0603 50V 100NP80M
2206	2238 586 59812	0603 50V 100NP80M
2207	2238 586 59812	0603 50V 100NP80M
2208	2238 586 59812	0603 50V 100NP80M
2209	2238 586 59812	0603 50V 100NP80M
2210	2238 586 59812	0603 50V 100NP80M
2211	2238 586 59812	0603 50V 100NP80M
2212	2238 586 59812	0603 50V 100NP80M
2213	2238 586 59812	0603 50V 100NP80M
2214	2238 586 59812	0603 50V 100NP80M
2215	2238 586 59812	0603 50V 100NP80M
2216	3198 017 41050	0603 10V 1µF COL R
2217	5322 126 11583	10nF 10% 50V 0603
2218	3198 017 41050	0603 10V 1µF COL R
2219	4822 122 33761	22pF 5% 50V
2220	4822 122 33761	22pF 5% 50V
2221	2238 586 59812	0603 50V 100NP80M
2223	2020 552 94427	0603 50V 100P PM5 R
2224	2020 552 94427	0603 50V 100P PM5 R
2225	2020 552 94427	0603 50V 100P PM5 R
2226	2020 552 94427	0603 50V 100P PM5 R
2227	2238 586 59812	0603 50V 100NP80M
2228	2238 586 59812	0603 50V 100NP80M
2229	2238 586 59812	0603 50V 100NP80M
2230	2238 586 59812	0603 50V 100NP80M
2231	2238 586 59812	0603 50V 100NP80M
2232	4822 126 13879	220nF 20% 16V
2234	4822 126 13617	1.8nF 10% 50V
2235	4822 126 14549	33nF 16V O6O3
2236	4822 126 13617	1.8nF 10% 50V
2237	2238 586 59812	0603 50V 100NP80M
2238	2238 586 59812	0603 50V 100NP80M
2239	2238 586 59812	0603 50V 100NP80M
2300	2238 586 59812	0603 50V 100NP80M
2301	2238 586 59812	0603 50V 100NP80M
2302	2238 586 59812	0603 50V 100NP80M
2303	2238 586 59812	0603 50V 100NP80M
2304	2238 586 59812	0603 50V 100NP80M
2305	2238 586 59812	0603 50V 100NP80M
2306	2238 586 59812	0603 50V 100NP80M
2307	2238 586 59812	0603 50V 100NP80M
2308	4822 126 13883	220pF 5% 50V
2309	4822 126 13883	220pF 5% 50V
2310	4822 126 13883	220pF 5% 50V
2311	2238 586 59812	0603 50V 100NP80M
2313	2238 586 59812	0603 50V 100NP80M
2315	2238 586 59812	0603 50V 100NP80M
2316	2238 586 59812	0603 50V 100NP80M
2320	4822 124 80151	47µF 16V
2321	4822 124 80151	47µF 16V
2402	2238 586 59812	0603 50V 100NP80M
2405	2238 586 59812	0603 50V 100NP80M
2408	2238 586 59812	0603 50V 100NP80M
2410	4822 124 12095	100µF 20% 16V
2411	4822 124 12095	100µF 20% 16V
2414	2238 586 59812	0603 50V 100NP80M
2415	3198 017 41050	0603 10V 1µF COL R
2417	4822 124 23002	10µF 16V
2418	3198 017 44740	0603 10V 470nF COL
2500	4822 124 80349	47µF 20% 6.3V
2501	2238 586 59812	0603 50V 100NP80M
2504	2238 586 59812	0603 50V 100NP80M
2505	2238 586 59812	0603 50V 100NP80M
2506	2238 586 59812	0603 50V 100NP80M
2507	2238 586 59812	0603 50V 100NP80M
2510	2238 586 59812	0603 50V 100NP80M
2511	2238 586 59812	0603 50V 100NP80M
2512	2238 586 59812	0603 50V 100NP80M
2513	2238 586 59812	0603 50V 100NP80M
2516	2238 586 59812	0603 50V 100NP80M
2517	2238 586 59812	0603 50V 100NP80M
2518	2238 586 59812	0603 50V 100NP80M
2519	2238 586 59812	0603 50V 100NP80M
2520	2238 586 59812	0603 50V 100NP80M
2522	4822 126 14247	0603 50V 1N5 COL R
2524	2238 586 59812	0603 50V 100NP80M
2525	4822 124 80349	47µF 20% 6.3V
2533	2238 586 59812	0603 50V 100NP80M
2604	4822 126 14494	22nF 10% 25V 0603
2605	4822 124 23002	10µF 16V
2606	2238 586 59812	0603 50V 100NP80M
2607	4822 124 23002	10µF 16V
2608	2238 586 59812	0603 50V 100NP80M
2619	2238 586 59812	0603 50V 100NP80M
2620	2238 586 59812	0603 50V 100NP80M
2621	2238 586 59812	0603 50V 100NP80M
2622	2238 586 59812	0603 50V 100NP80M
2623	2238 586 59812	0603 50V 100NP80M
2624	2238 586 59812	0603 50V 100NP80M
2625	2238 586 59812	0603 50V 100NP80M
2626	2238 586 59812	0603 50V 100NP80M
2627	2238 586 59812	0603 50V 100NP80M
2628	2238 586 59812	0603 50V 100NP80M
2629	2238 586 59812	0603 50V 100NP80M
2630	2238 586 59812	0603 50V 100NP80M
2631	2238 586 59812	0603 50V 100NP80M
2632	2238 586 59812	0603 50V 100NP80M
2633	2238 586 59812	0603 50V 100NP80M
2634	2238 586 59812	0603 50V 100NP80M
2635	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2636	3198 030 74780	EL SM 35V 4U7 PM20 COL R
2637	2238 586 59812	0603 50V 100NP80M
2638	2020 552 94427	0603 50V 100P PM5 R
2700	2238 586 59812	0603 50V 100NP80M
2701	4822 126 11785	0603 50V 47P PM5
2702	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2703	4822 126 11785	0603 50V 47P PM5
2704	4822 126 11785	0603 50V 47P PM5
2705	4822 126 11785	0603 50V 47P PM5
2706	4822 124 12095	100µF 20% 16V
2707	2238 586 59812	0603 50V 100NP80M
2708	2238 586 59812	0603 50V 100NP80M
2709	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2710	2238 586 59812	0603 50V 100NP80M
2711	4822 126 11785	0603 50V 47P PM5
2712	4822 126 11785	0603 50V 47P PM5
2713	4822 124 12095	100µF 20% 16V
2714	2238 586 59812	0603 50V 100NP80M
2715	3198 016 31020	0603 25V 1nF
2716	3198 016 31020	0603 25V 1nF
2718	2238 586 59812	0603 50V 100NP80M
2720	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2721	4822 126 11785	0603 50V 47P PM5
2722	4822 126 11785	0603 50V 47P PM5
2723	2238 586 59812	0603 50V 100NP80M
2724	2238 586 59812	0603 50V 100NP80M
2725	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2726	4822 126 11785	0603 50V 47P PM5
2727	4822 126 11785	0603 50V 47P PM5
2728	4822 124 23002	10µF 16V
2729	4822 124 12095	100µF 20% 16V
2730	2238 586 59812	0603 50V 100NP80M
2731	2238 586 59812	0603 50V 100NP80M
2732	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2733	4822 126 11785	0603 50V 47P PM5
2734	4822 126 11785	0603 50V 47P PM5
2735	2238 586 59812	0603 50V 100NP80M
2736	2238 586 59812	0603 50V 100NP80M
2737	2238 586 59812	0603 50V 100NP80M
2738	4822 122 33761	22pF 5% 50V
2739	2238 586 59812	0603 50V 100NP80M
2740	4822 124 12095	100µF 20% 16V
2741	2238 586 59812	0603 50V 100NP80M
2742	3198 030 82280	EL SM 50V 2U2 PM20 COL R
2743	4822 126 11785	0603 50V 47P PM5
2744	4822 126 11785	0603 50V 47P PM5
2745	2238 586 59812	0603 50V 100NP80M
2746	2238 586 59812	0603 50V 100NP80M
2747	4822 124 23002	10µF 16V
2748	4822 124 12095	100µF 20% 16V
2749	2238 586 59812	0603 50V 100NP80M
2750	2238 586 59812	0603 50V 100NP80M
2751	4822 124 12095	100µF 20% 16V
2800	2238 586 59812	0603 50V 100NP80M
2801	2238 586 59812	0603 50V 100NP80M
2802	2238 586 59812	0603 50V 100NP80M
2803	2238 586 59812	0603 50V 100NP80M
2804	2238 586 59812	0603 50V 100NP80M
2805	2238 586 59812	0603 50V 100NP80M
2806	2238 586 59812	0603 50V 100NP80M
2807	2238 586 59812	0603 50V 100NP80M
2808	2238 586 59812	0603 50V 100NP80M
2809	2238 586 59812	0603 50V 100NP80M
2810	4822 126 14238	0603 50V 2N2 COL R
2811	5322 126 11583	10nF 10% 50V 0603
2813	4822 126 14225	56pF 5% 50V 0603
2814	2238 586 59812	0603 50V 100NP80M
2816	2238 586 59812	0603 50V 100NP80M
2817	5322 126 11578	1nF 10% 50V 0603
2900	4822 124 12095	100µF 20% 16V
2901	2238 586 59812	0603 50V 100NP80M
2902	5322 126 11583	10nF 10% 50V 0603
2903	4822 122 33761	22pF 5% 50V
2904	4822 122 33761	22pF 5% 50V
2907	2238 586 59812	0603 50V 100NP80M
2908	2238 586 59812	0603 50V 100NP80M
2915	4822 122 33761	22pF 5% 50V
2918	5322 126 11583	10nF 10% 50V 0603
2919	5322 126 11583	10nF 10% 50V 0603

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3003	4822 051 30103	10k 5% 0.062W
3008	4822 051 30103	10k 5% 0.062W
3010	4822 051 30103	10k 5% 0.062W
3019	4822 051 30339	33Ω 5% 0.062W
3020	4822 051 30339	33Ω 5% 0.062W
3021	4822 051 30339	33Ω 5% 0.062W
3022	4822 051 30339	33Ω 5% 0.062W
3023	4822 051 30339	33Ω 5% 0.062W
3024	4822 051 30339	33Ω 5% 0.062W
3026	4822 051 30339	33Ω 5% 0.062W

3027	4822 051 30339	33Ω 5% 0.062W
3028	4822 051 30339	33Ω 5% 0.062W
3029	4822 051 30339	33Ω 5% 0.062W
3030	4822 051 30339	33Ω 5% 0.062W
3036	4822 051 30103	10k 5% 0.062W
3037	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3100	4822 051 30563	56k 5% 0.062W
3101	4822 051 30102	1k 5% 0.062W
3102	4822 051 30223	22k 5% 0.062W
3103	4822 051 30102	1k 5% 0.062W
3104	5322 117 13028	12k 1% 0.063W 0603 RC22H
3105	4822 117 13501	82Ω 5% 0.62W 0603
3106	4822 051 30221	220Ω 5% 0.062W
3107	4822 117 13501	82Ω 5% 0.62W 0603
3108	4822 051 30222	2k2 5% 0.062W
3110	4822 051 30683	68k 5% 0.062W
3111	4822 051 30221	220Ω 5% 0.062W
3112	4822 051 30103	10k 5% 0.062W
3113	4822 051 30333	33k 5% 0.062W
3114	4822 117 12903	1k8 1% 0.063W 0603
3116	4822 051 30102	1k 5% 0.062W
3117	4822 051 30391	390Ω 5% 0.062W
3118	4822 051 30103	10k 5% 0.062W
3119	4822 051 30103	10k 5% 0.062W
3120	4822 051 30103	10k 5% 0.062W
3121	4822 051 30103	10k 5% 0.062W
3122	2322 704 69109	
3123	4822 051 30103	10k 5% 0.062W
3124	4822 051 20228	2Ω2 5% 0.1W
3125	4822 051 30103	10k 5% 0.062W
3126	4822 117 12139	22Ω 5% 0.062W
3127	4822 051 30103	10k 5% 0.062W
3128	4822 051 30474	470k 5% 0.062W
3129	4822 051 30221	220Ω 5% 0.062W
3130	4822 051 30222	2k2 5% 0.062W
3131	4822 051 30682	6k8 5% 0.062W
3132	2322 704 69109	
3133	4822 051 30472	4k7 5% 0.062W
3134	4822 051 30472	4k7 5% 0.062W
3136	4822 117 13632	100k 1% 0603 0.62W
3138	4822 051 30103	10k 5% 0.062W
3142	4822 051 30008	0Ω jumper
3143	4822 051 30008	0Ω jumper
3144	4822 051 30008	0Ω jumper
3145	4822 051 30008	0Ω jumper
3146	4822 051 30008	0Ω jumper
3147	4822 051 30008	0Ω jumper
3152	4822 051 30223	22k 5% 0.062W
3153	4822 117 12139	22Ω 5% 0.062W
3154	4822 051 30223	22k 5% 0.062W
3155	4822 117 12139	22Ω 5% 0.062W
3156	4822 051 30101	100Ω 5% 0.062W
3157	4822 051 30101	100Ω 5% 0.062W
3158	4822 051 30393	39k 5% 0.062W
3159	4822 117 12968	820Ω 5% 0.62W
3160	4822 051 30393	39k 5% 0.062W
3161	4822 117 12968	820Ω 5% 0.62W
3162	4822 051 30101	100Ω 5% 0.062W
3163	4822 051 30101	100Ω 5% 0.062W
3200	4822 051 30223	22k 5% 0.062W
3202	4822 051 30102	1k 5% 0.062W
3204	4822 051 30223	22k 5% 0.062W
3205	4822 051 30223	22k 5% 0.062W
3207	4822 051 30102	1k 5% 0.062W
3209	4822 051 30223	22k 5% 0.062W
3210	4822 051 30223	22k 5% 0.062W
3212	4822 051 30223	22k 5% 0.062W
3214	4822 051 30472	4k7 5% 0.062W
3216	4822 051 30223	22k 5% 0.062W
3218	4822 051 30223	22k 5% 0.062W
3219	4822 051 30472	4k7 5% 0.062W
3222	4822 051 30223	22k 5% 0.062W
3223	4822 051 30223	22k 5% 0.062W
3226	4822 051 30102	1k 5% 0.062W
3227	4822 051 30223	22k 5% 0.062W
3229	3198 031 11010	RST NETW 1206 4X100Ω PM5 COL R
3236	4822 051 30472	4k7 5% 0.062W
3237	4822 051 30102	1k 5% 0.062W
3239	4822 117 12891	220k 1% ERJ3Ω
3241	4822 051 30102	1k 5% 0.062W
3242	4822 051 30223	22k 5% 0.062W
3245	4822 051 30101	100Ω 5% 0.062W
3246	4822 051 30101	100Ω 5% 0.062W
3247	4822 051 30331	330Ω 5% 0.062W
3250	4822 117 13525	24k 1% 0.62W RC22H 0603
3251	4822 051 30103	10k 5% 0.062W
3255	4822 051 30151	150Ω 5% 0.062W
3256	4822 051 30101	100Ω 5% 0.062W
3257	4822 117 13573	NETW 4 X 47Ω 5% MNR14
3263	4822 051 30103	10k 5% 0.062W
3266	4822 051 30103	10k 5% 0.062W
3267	4822 051 30392	3k9 5% 0.063W 0603
3268	4822 051 30272	2k7 5% 0.062W
3270	4822 051 30392	3k9 5% 0.063W 0603
3271	4822 051 30103	10k 5% 0.062W
3272	4822 051 30103	10k 5% 0.062W
3273	4822 051 30103	10k 5% 0.062W
3274	4822 051 30103	10k 5% 0.062W
3275	4822 051 30472	4k7 5% 0.062W
3277	4822 051 30479	47Ω 5% 0.062W
3278	4822 051 30103	10k 5% 0.062W
3279	4822 051 30103	10k 5% 0.062W
3280	4822 051 30472	4k7 5% 0.062W
3282	4822 051 30472	4k7 5% 0.062W
3287	4822 051 30008	0Ω jumper
3288	4822 051 30103	10k 5% 0.062W
3289	4822 051 30103	10k 5% 0.062W
3290	4822 051 30103	10k 5% 0.062W
3291	4822 051 30103	10k 5% 0.062W
3294	4822 051 30479	47Ω 5% 0.062W
3300	4822 051 20108	1Ω 5% 0.1W
3301	4822 051 20108	1Ω 5% 0.1W
3304	4822 117 13501	82Ω 5% 0.62W 0603
3306	4822 117 13632	100k 1% 0603 0.62W
3307	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3308	4822 117 13501	82Ω 5% 0.62W 0603
3309	5322 117 13026	4k7 1% 0.063W 0603 RC22H
3310	4822 051 30273	27k 5% 0.062W
3312	4822 117 13632	100k 1% 0603 0.62W
3313	4822 051 30273	27k 5% 0.062W
3315	4822 051 20228	2Ω2 5% 0.1W
3316	4822 051 20228	2Ω2 5% 0.1W
3319	4822 117 13632	100k 1% 0603 0.62W
3321	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3322	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
3323	4822 051 30103	10k 5% 0.062W
3324	4822 051 30153	15k 5% 0.062W
3325	4822 051 30123	12k 5% 0.062W
3326	4822 051 20228	2Ω2 5% 0.1W
3327	4822 051 20228	2Ω2 5% 0.1W
3328	4822 051 30153	15k 5% 0.062W
3332	4822 051 30682	6k8 5% 0.062W
3333	4822 051 30682	6k8 5% 0.062W
3334	4822 051 30682	6k8 5% 0.062W
3336	4822 051 20008	0Ω jumper . (0805)
3337	4822 051 20008	0Ω jumper . (0805)
3340	4822 051 30153	15k 5% 0.062W
3341	4822 051 30272	2k7 5% 0.062W
3342	4822 051 30008	0Ω jumper
3343	4822 117 12917	1Ω 5% 0.062W CASE0603
3401	4822 051 30103	10k 5% 0.062W
3402	4822 117 13632	100k 1% 0603 0.62W
3403	4822 051 30103	10k 5% 0.062W
3404	4822 051 30223	22k 5% 0.062W
3405	4822 051 30222	2k2 5% 0.062W
3406	4822 051 30223	22k 5% 0.062W
3407	4822 051 30103	10k 5% 0.062W
3409	4822 051 30103	10k 5% 0.062W
3411	4822 051 30223	22k 5% 0.062W
3412	4822 051 30472	4k7 5% 0.062W
3413	4822 051 30223	22k 5% 0.062W
3414	4822 051 30223	22k 5% 0.062W
3501	4822 051 30102	1k 5% 0.062W
3502	4822 051 30103	10k 5% 0.062W
3503	4822 051 30472	4k7 5% 0.062W
3504	4822 051 30472	4k7 5% 0.062W
3505	4822 051 30103	10k 5% 0.062W
3506	4822 051 30103	10k 5% 0.062W
3507	4822 051 30103	10k 5% 0.062W
3508	4822 051 30102	1k 5% 0.062W
3509	4822 051 30101	100Ω 5% 0.062W
3510	4822 051 30103	10k 5% 0.062W
3512	4822 051 30682	6k8 5% 0.062W
3531	4822 051 30472	4k7 5% 0.062W
3604	4822 051 30332	3k3 5% 0.062W
3605	4822 051 30332	3k3 5% 0.062W
3606	4822 051 30103	10k 5% 0.062W
3607	4822 051 30103	10k 5% 0.062W
3608	4822 051 30103	10k 5% 0.062W
3609	4822 051 30561	560Ω 5% 0.062W
3611	4822 051 30479	47Ω 5% 0.062W
3612	4822 051 30479	47Ω 5% 0.062W
3613	4822 051 30103	10k 5% 0.062W
3621	4822 051 30103	10k 5% 0.062W
3622	4822 051 30101	100Ω 5% 0.062W
3623	4822 051 30479	47Ω 5% 0.062W
3624	4822 051 30101	100Ω 5% 0.062W
3625	4822 051 30103	10k 5% 0.062W
3626	4822 051 30332	3k3 5% 0.062W
3627	4822 051 30332	3k3 5% 0.062W
3628	4822 051 30103	10k 5% 0.062W
3629	4822 051 30332	3k3 5% 0.062W
3630	4822 051 30332	3k3 5% 0.062W
3631	4822 051 30101	100Ω 5% 0.062W
3632	4822 051 30101	100Ω 5% 0.062W
3633	4822 051 30339	33Ω 5% 0.062W
3634	4822 051 30339	33Ω 5% 0.062W
3635	4822 051 30339	33Ω 5% 0.062W
3636	4822 051 30339	33Ω 5% 0.062W
3642	2322 704 61303	RST SM 0603 RC22H 13k PM1 R
3643	2322 704 61303	RST SM 0603 RC22H 13k PM1 R
3644	4822 051 30101	100Ω 5% 0.062W
3645	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3646	5322 117 13042	3k9 1% 0.063W 0603 RC22H
3647	4822 051 30479	47Ω 5% 0.062W
3648	4822 051 30103	10k 5% 0.062W
3702	4822 051 30332	3k3 5% 0.062W
3703	4822 051 30332	3k3 5% 0.062W
3704	4822 051 30683	68k 5% 0.062W
3705	4822 051 30471	470Ω 5% 0.062W
3706	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3707	4822 051 30101	100Ω 5% 0.062W
3708	4822 051 30221	220Ω 5% 0.062W
3709	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3710	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3711	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3712	4822 117 12925	47k 1% 0.063W 0603
3713	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3714	4822 051 30221	220Ω 5% 0.062W
3715	4822 051 30683	68k 5% 0.062W
3716	4822 051 30471	470Ω 5% 0.062W
3717	4822 051 30101	100Ω 5% 0.062W
3718	4822 051 30221	220Ω 5% 0.062W
3719	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3720	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3721	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3722	4822 117 12925	47k 1% 0.063W 0603
3723	4822 051 30221	220Ω 5% 0.062W
3726	4822 051 30683	68k 5% 0.062W
3727	4822 051 30471	470Ω 5% 0.062W
3728	4822 051 30101	100Ω 5% 0.062W
3729	4822 051 30221	220Ω 5% 0.062W
3730	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3731	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3732	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3733	4822 117 12925	47k 1% 0.063W 0603
3734	4822 051 30221	220Ω 5% 0.062W
3735	4822 051 30683	68k 5% 0.062W
3736	4822 051 30471	470Ω 5% 0.062W
3737	4822 051 30101	100Ω 5% 0.062W
3738	4822 051 30221	220Ω 5% 0.062W
3739	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3740	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3741	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3742	4822 117 12925	47k 1% 0.063W 0603
3743	4822 051 30221	220Ω 5% 0.062W
3744	4822 051 30683	68k 5% 0.062W
3745	4822 051 30471	470Ω 5% 0.062W
3746	4822 051 30101	100Ω 5% 0.062W
3747	4822 051 30221	220Ω 5% 0.062W
3748	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3749	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3750	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3751	4822 117 12925	47k 1% 0.063W 0603
3752	4822 051 30221	220Ω 5% 0.062W
3753	4822 117 12139	22Ω 5% 0.062W
3754	4822 051 30683	68k 5% 0.062W
3755	4822 051 30471	470Ω 5% 0.062W
3756	4822 051 30101	100Ω 5% 0.062W
3757	4822 051 30221	220Ω 5% 0.062W
3758	4822 051 30689	68Ω 5% 0.063W 0603 RC21 RST SM
3759	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3760	5322 117 13059	560Ω 1% 0.063W 0603 RC22H
3761	4822 117 12925	47k 1% 0.063W 0603
3762	4822 051 30221	220Ω 5% 0.062W
3763	3198 031 11010	RST NETW 1206 4X100Ω PM5 COL R

3764	4822 051 30479	47Ω 5% 0.062W
3765	4822 051 30479	47Ω 5% 0.062W
3766	4822 051 30332	3k3 5% 0.062W
3767	4822 051 30332	3k3 5% 0.062W
3772	4822 051 20008	0Ω jumper . (0805)
3773	4822 051 20008	0Ω jumper . (0805)
3775	4822 051 20008	0Ω jumper . (0805)
3800	4822 051 30339	33Ω 5% 0.062W
3801	4822 051 30392	3k9 5% 0.063W 0603
3802	4822 051 30392	3k9 5% 0.063W 0603
3803	4822 117 12139	22Ω 5% 0.062W
3805	5322 117 13062	390Ω 1% 0.063W 0603 RC22H
3806	4822 051 30123	12k 5% 0.062W
3807	4822 051 30682	6k8 5% 0.062W
3808	4822 051 30339	33Ω 5% 0.062W
3813	4822 051 30103	10k 5% 0.062W
3816	4822 051 30339	33Ω 5% 0.062W
3900	4822 051 30103	10k 5% 0.062W
3901	4822 051 30103	10k 5% 0.062W
3902	4822 051 30339	33Ω 5% 0.062W
3903	4822 051 30569	56Ω 5% 0.062W
3904	4822 051 30569	56Ω 5% 0.062W
3905	4822 051 30339	33Ω 5% 0.062W
3906	4822 051 30332	3k3 5% 0.062W
3907	4822 051 30479	47Ω 5% 0.062W
3910	4822 051 30339	33Ω 5% 0.062W
4xxx	4822 051 10008	0Ω 5% 0.25W (1206)
4xxx	4822 051 20008	0Ω 5% 0.25W (0805)

5100	4822 157 11499	BLM11P600SPT
5101	4822 157 11499	BLM11P600SPT
5102	4822 157 11499	BLM11P600SPT
5200	4822 157 11499	BLM11P600SPT
5201	4822 157 11499	BLM11P600SPT
5202	4822 157 11499	BLM11P600SPT
5203	4822 157 11499	BLM11P600SPT
5300	4822 157 11499	BLM11P600SPT
5301	4822 157 11499	BLM11P600SPT
5302	4822 157 11499	BLM11P600SPT
5401	4822 157 11499	BLM11P600SPT
5402	4822 157 11499	BLM11P600SPT
5502	4822 157 71206	BLM21A601SPT
5504	2422 549 43303	IND FXD SM EMI 100mH z 600R R
5505	4822 157 71206	BLM21A601SPT
5600	4822 157 11499	BLM11P600SPT
5601	4822 157 11499	BLM11P600SPT
5602	4822 157 11499	BLM11P600SPT
5603	4822 157 11499	BLM11P600SPT
5700	4822 157 11499	BLM11P600SPT
5701	4822 157 70651	12µH (NL322522T-120J)
5702	4822 157 11499	BLM11P600SPT
5703	4822 157 11499	BLM11P600SPT
5704	4822 157 11717	BLM31P500SPT
5705	4822 157 11499	BLM11P600SPT
5706	4822 157 70651	12µH (NL322522T-120J)
5707	4822 157 11499	BLM11P600SPT
5708	4822 157 11717	BLM31P500SPT
5712	4822 157 70651	12µH (NL322522T-120J)
5713	4822 157 11499	BLM11P600SPT
5714	4822 157 11499	BLM11P600SPT
5715	4822 157 70651	12µH (NL322522T-120J)
5716	4822 157 11717	BLM31P500SPT
5717	4822 157 11499	BLM11P600SPT
5718	4822 157 11499	BLM11P600SPT
5719	4822 157 11499	BLM11P600SPT
5720	4822 157 11499	BLM11P600SPT
5721	4822 157 11499	BLM11P600SPT
5722	4822 157 70651	12µH (NL322522T-120J)
5723	4822 157 11499	BLM11P600SPT
5724	4822 157 70651	12µH (NL322522T-120J)
5801	4822 157 11499	BLM11P600SPT
5901	2422 549 43303	IND FXD SM EMI 100mH z 600R R
5902	2422 549 43303	IND FXD SM EMI 100mH z 600R R
5904	2422 549 43303	IND FXD SM EMI 100mH z 600R R
5905	2422 549 43303	IND FXD SM EMI 100mH z 600R R

6100	4822 130 11397	BAS316
6101	4822 130 11397	BAS316
6300	9322 128 69685	S1D
6301	9322 128 69685	S1D
6302	9322 128 69685	S1D
6400	4822 130 11397	BAS316

7100	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7101	4822 209 32073	MC34072D
7102	4822 209 90927	L78L05ACD
7103	5322 130 60159	BC846B
7105	9352 703 49118	IC SM TZA1033HL/K2 (PHSE) R
7106	4822 209 32073	MC34072D
7107	5322 130 60845	BC807-25
7108	4822 130 42804	BC817-25
7109	9337 331 10215	FET SIG SM BST82 (PHSE) R
7110	5322 130 42718	BFS20
7111	5322 130 42718	BFS20
7200	9322 163 27685	IC SM NCP301LSN45 (ONSE) R
7201	4822 130 60373	BC856B
7202	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7207	9352 681 05557	IC SM SAA7812HL/M3B (PHSE) Y
7300	9322 139 85668	BA6665FM
7301	4822 209 30095	LM833D
7303	4822 209 17229	BA5938FM
7305	9322 136 29668	L78M09CDT
7400	9322 130 41668	IC SM M24C64-WMN6 (ST00) R
7404	5322 130 60159	BC846B
7405	5322 130 60159	BC846B
7406	9352 499 80118	IC SM 74LVC00APW (PHSE) R
7409	5322 130 60159	BC846B
7412	9322 178 88685	IC SM NCP301LSN27 (ONSE) R
7413	4822 130 60373	BC856B
7500	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRN0)R
7502	9322 166 67668	IC SM MT48LC4M16A2TG-7E(MRN0)R
7508	9340 425 20115	TRA SIG SM BC847BS (PHSE) R
7601	9322 181 01671	IC SM STI5580EVB (ST00) Y
7700	9965 000 04199	BSN20
7701	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7703	9965 000 04199	BSN20
7704	9322 142 88668	IC SM LF25CDT (ST00) R
7705	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7707	9322 142 88668	IC SM LF25CDT (ST00) R
7709	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7713	9322 179 78668	IC SM LF18ABDT (ST00) R
7714	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7716	4822 209 17398	LD1117DT33
7717	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7719	4822 209 17398	LD1117DT33
7720	9352 456 80115	74HCT1G125GW
7721	9340 425 30115	TRA SIG SM BC847BPN (PHSE) R
7800	9352 708 12557	IC SM SAA7893HL/C2 (PHSE) Y
7801	5322 130 42718	BFS20
7803	9352 317 20118	IC SM 74LVC125APW (PHSE) R
7901	9322 151 71668	IC SM MK2703STR (MICL) R
7902	9322 184 32668	IC SM ICS612G-01 (ICSI) R
7904	9351 742 20118	IC SM 74HCT04PW (PHSE) R

Module SD4.00SA_CH

Various

0001	9305 023 61114	VAL6011/14